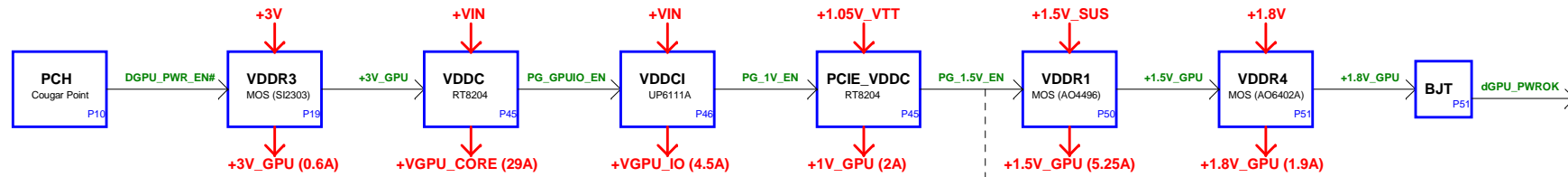


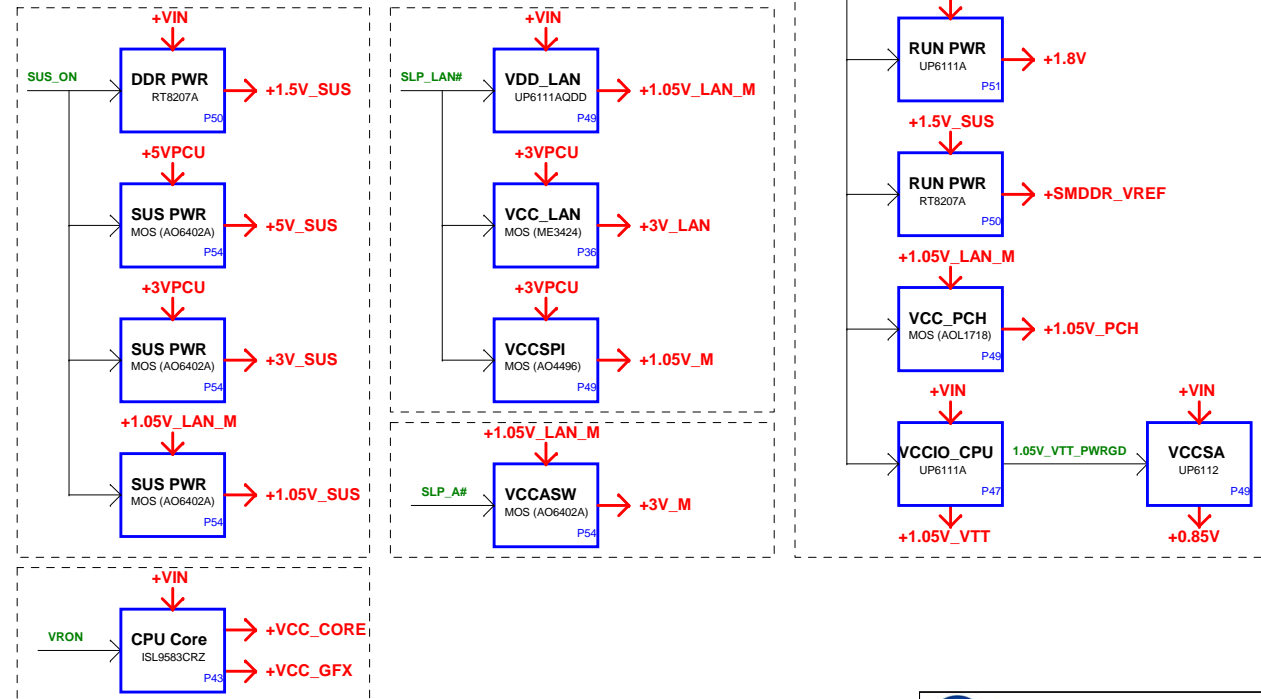
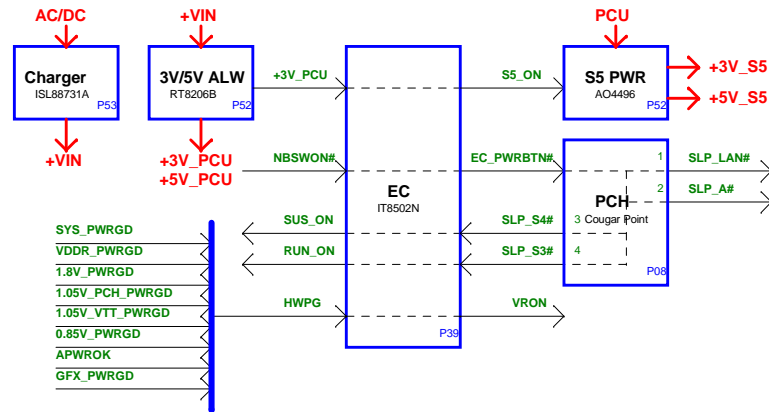
POWER	
Discharge	PG 38
RUN POWER SW 3VSUS, 5VSUS, 3V_S5, 5V_S5 +3V, +5V	PG 38
AC/BATT CONNECTOR	PG 42
BATT CHARGER	PG 39
REGULATOR (DDR3) 1.5VSUS, 0.75VSMDDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU	PG 40
REGULATOR +1.05V_VTT,+1.8V	PG 41
DC/DC 3VPCU, 5VPCU, +15V	PG 42
CPU Core	PG 43
VGA Core Discrete 1.8V_GPU, 1V_GFX_PCIE	PG 44
VGA Core UMA	PG 45

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)

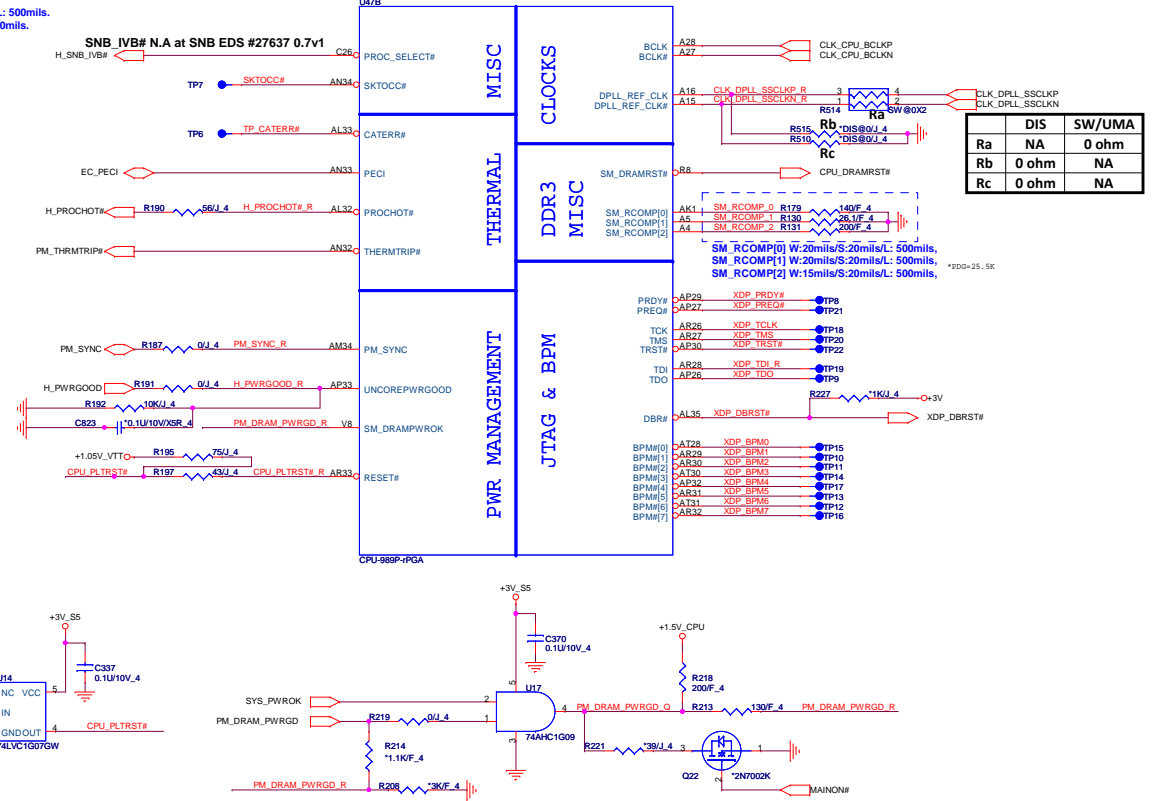


Main Power Rails

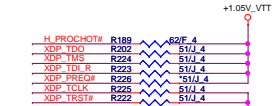
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+0.75V_DDR_VTT	+0.75V	DDR3 reference voltage	RUN_ON	
+0.85V	+0.9V	Intel new power rail	1.05V_VTT_PWRGD	
+1.05V_LAN_M	+1.05V	LAN M power for iAMT	SLP_LAN#	
+1.05V_M	+1.05V	ME power for iAMT	SLP_A#	
+1.05V_PCH	+1.05V	PCH core power	RUN_ON	
+1.05V_SUS	+1.05V	USB3.0 chip power	SUSD	
+1.05V_VTT	+1.05V	CPU core logic power	RUN_ON	
+1.5V	+1.5V	I/O module power	RUN_ON	
+1.5V_CPU	+1.5V	CPU DDR3 controller power	RUN_ON_D	
+1.5V_GPU	+1.5V	GPU DDR3 controller power	PG_1.5V_EN	
+1.5V_SUS	+1.5V	DDR3 SODIMM power	SUS_ON	
+1.8V	+1.8V	CPU/PCH/LVDS power	RUN_ON	
+1.8_GPU	+1.8V	GPU power	+1.5V_GPU	
+1V_GPU	+1V	GPU PCIE VDDC power	PG_1V_EN	
+3V	+3.3V	I/O power	RUN_ON	
+3V_GPU	+3.3V	GPU power	DGPU_PWR_EN#	
+3V_M	+3.3V	PCH/SPI power for iAMT	SLP_A#	
+3V_S5	+3.3V	3V power sequence	S5_ON	
+3V_SUS	+3.3V	USB3.0 chip power	SUSD	
+3VPCU	+3.3V	Always power	SYS_SHDN#	
+5V	+5V	I/O power	RUN_ON	
+5V_S5	+5V	5V power sequence	S5_ON	
+5V_SUS	+5V	USB2.0 power	SUSD	
+5VPCU	+5V	Always power	SYS_SHDN#	
+15V_ALW	+15V	Power sequence		
+SMDDR_VREF	+0.75V	DDR3 reference power	RUN_ON	
+VCC_CORE	+1.1V	CPU Core power	VRON	
+VCC_GFX	+1.52V	Internal GPU Core power	VRON	
+VGPU_CORE	+1V	GPU Core power	DGPU_VRON	
+VGPU_IO	+1V	GPU I/O controller power	PG_GPUIO_EN	
+19V		C power input		



Sandy Bridge Processor (CLK,MISC,JTAG)



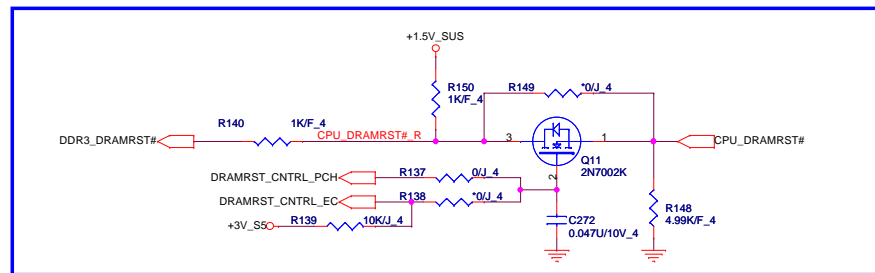
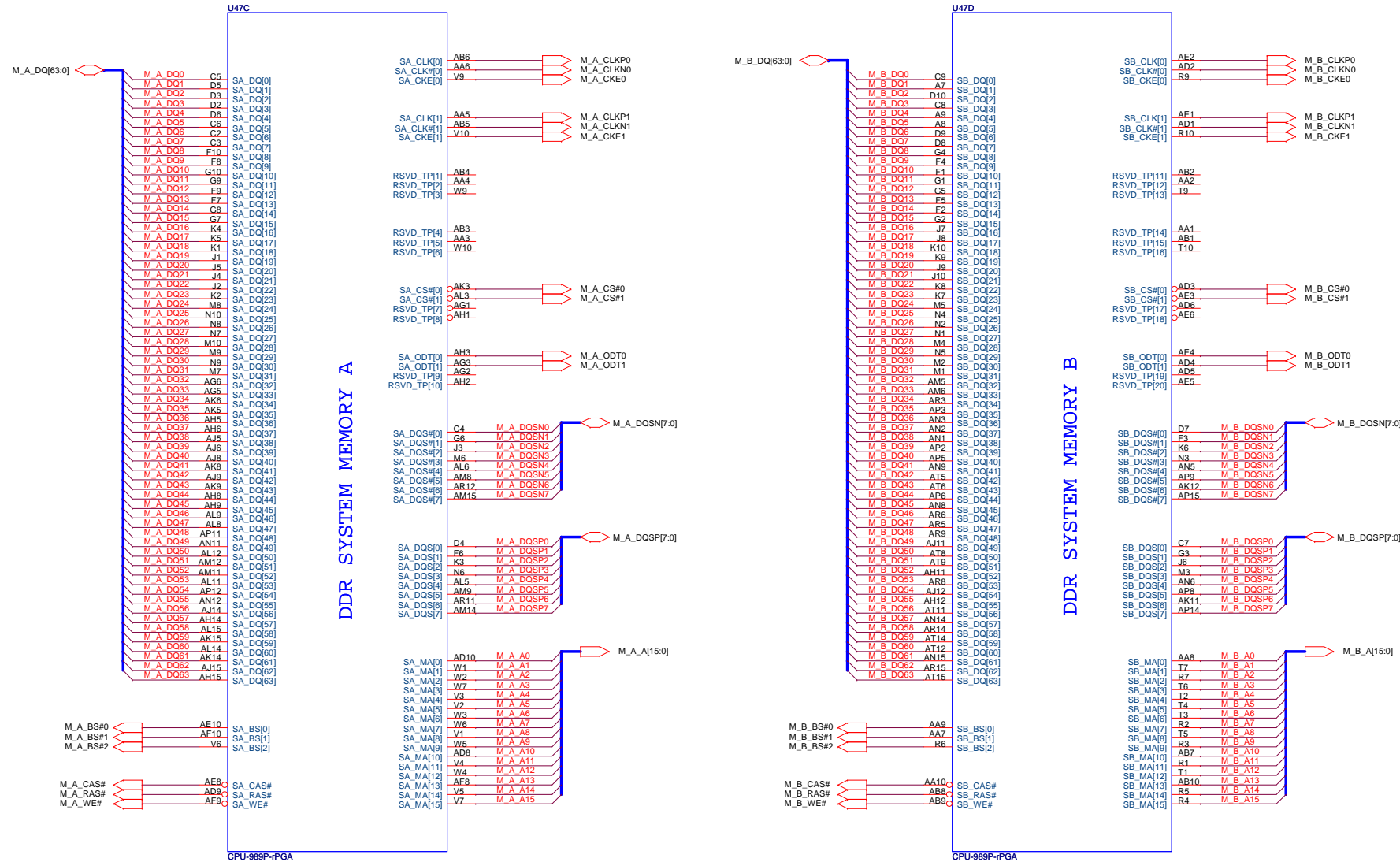
Processor pull-up(CPU)



Size	Document Number Sandy Bridge 1/4	Rev 1A
Date: Thursday, September 30, 2010	Sheet 4 of 48	

Sandy Bridge Processor (DDR3)

05



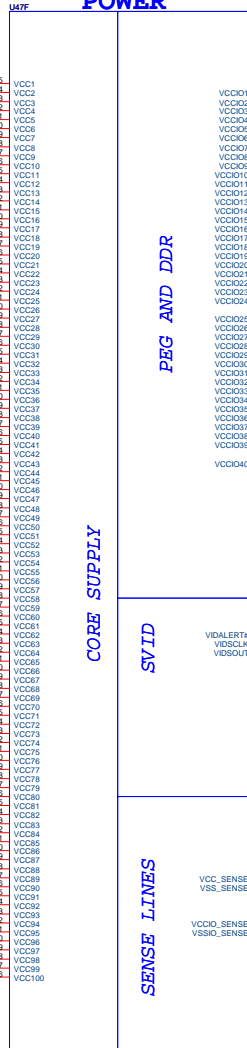
Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
 SNB 45W:55A
 22uF x 32
 22uF x 3 (Non-stuff)

POWER

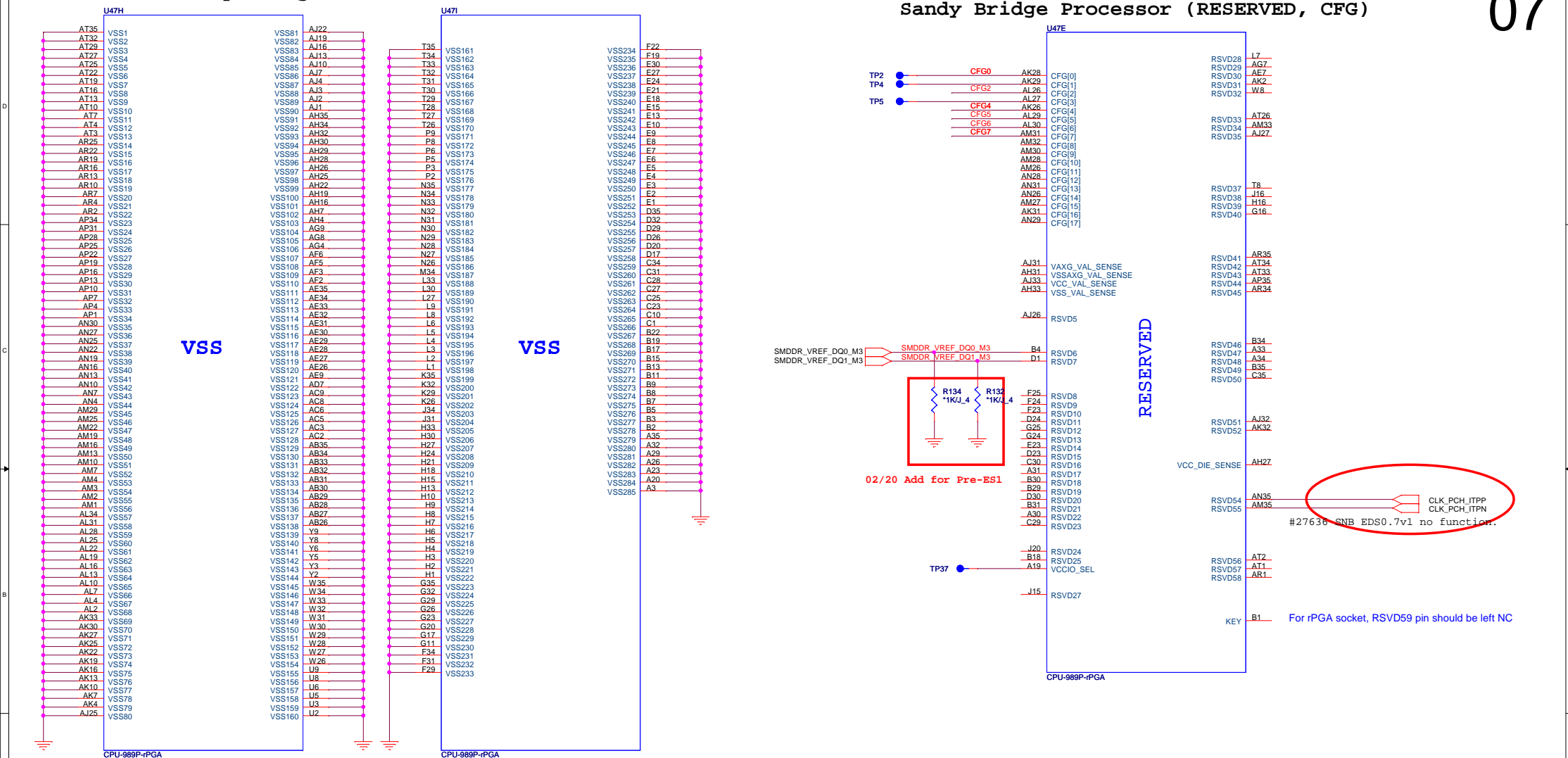
+VCC_CORE



Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP Leave NC for disable	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)

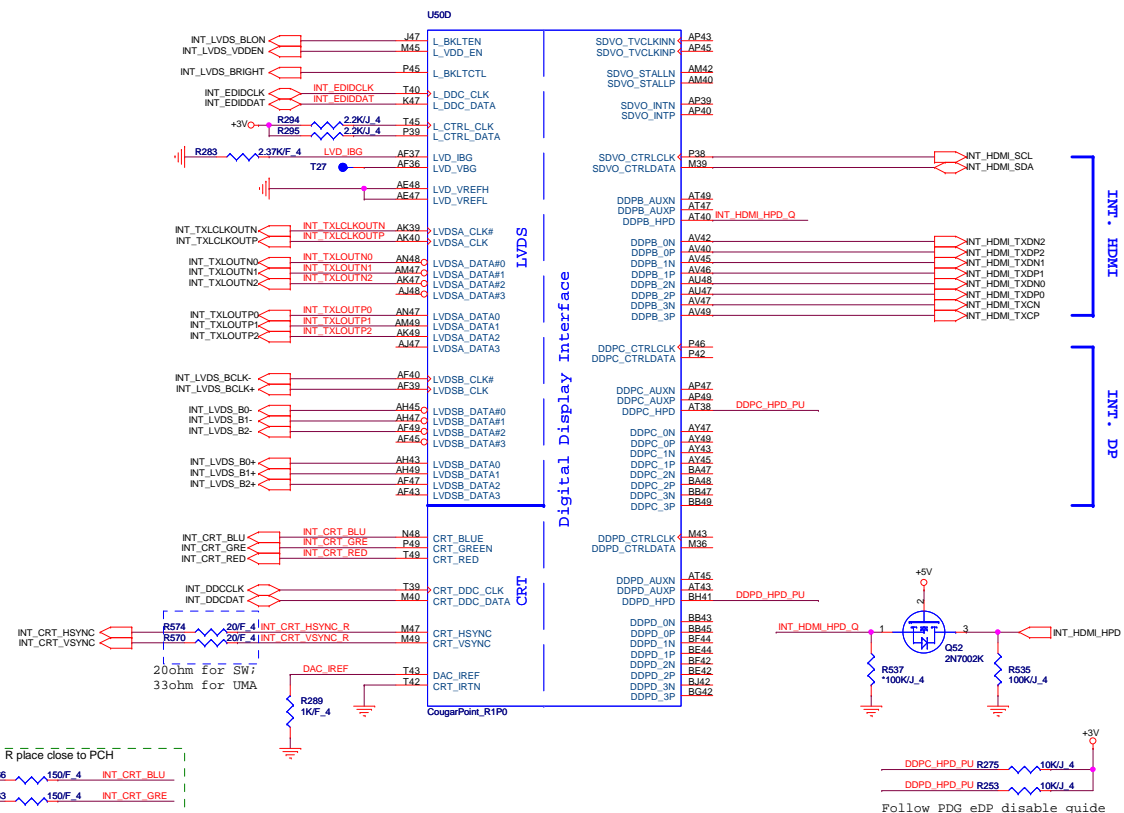
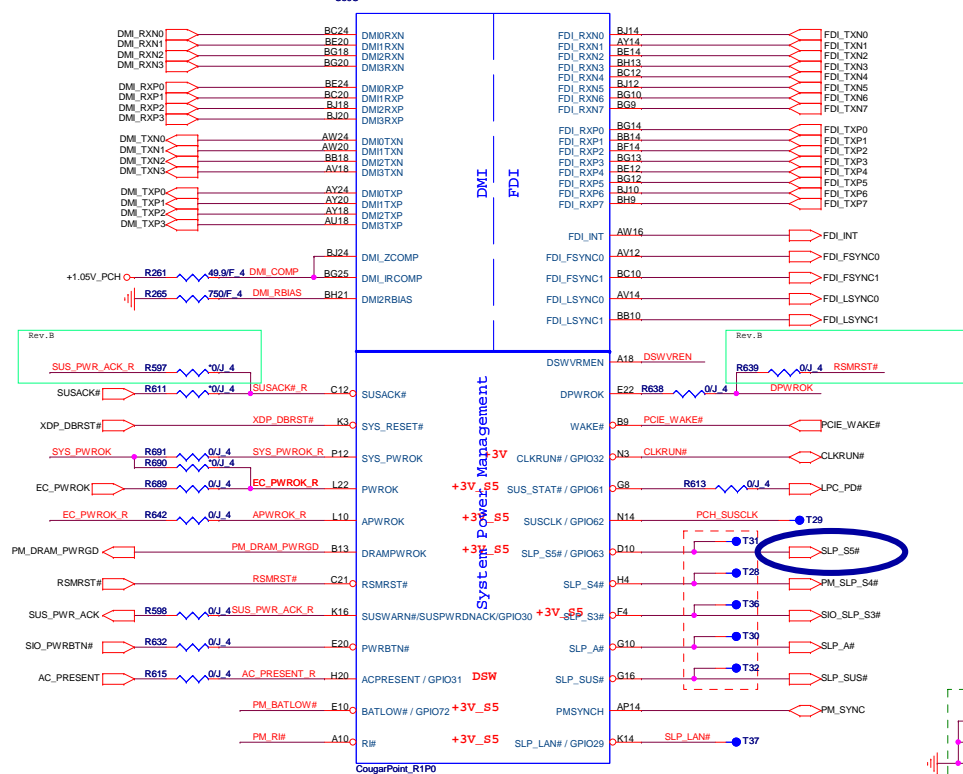
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : KL2D
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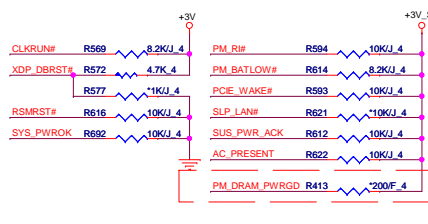
Size Document Number Rev 1A
Sandy Bridge 4/4

Date: Thursday, September 30, 2010 Sheet 7 of 48

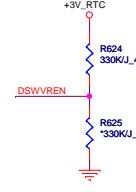
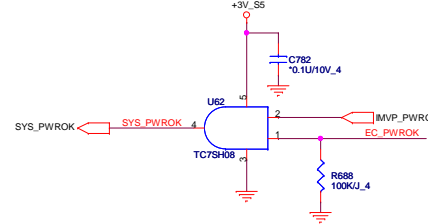
U50C



System PWR_OK(CLG)

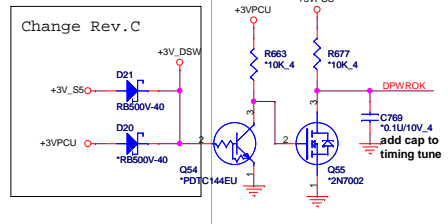


3/16 Change topology: 200ohm PU to +3V S5



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DPWROK FOR DSW



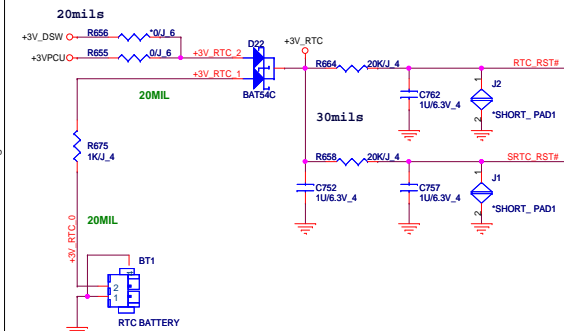
Deep sleep option	Support	Not support
SUS_PWR_ACK	To PCH SUSACK# (Pop R597)	EC or NC (Non-pop R597)
DPWROK	DSWPWRGD (Pop Q54, R663, Q55, R677)	RSMRST (Pop R639)
SLP_SUS	EC	NC



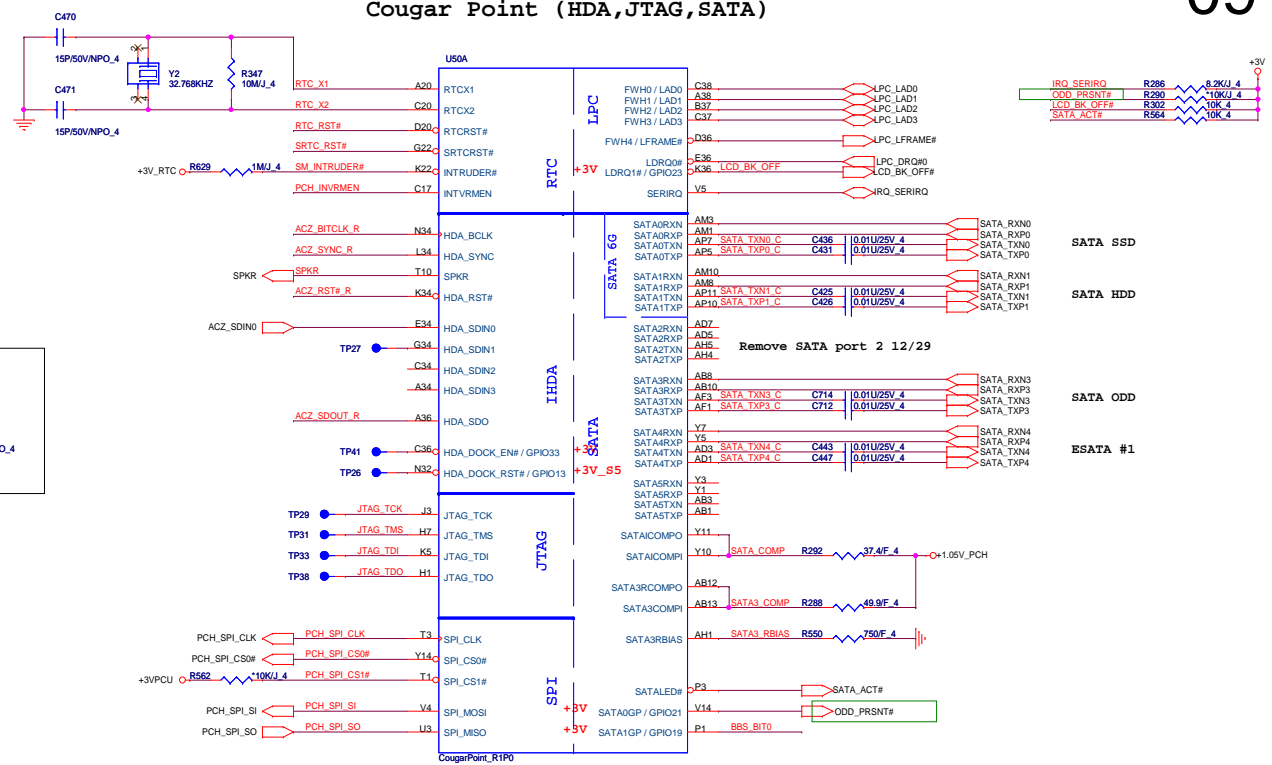
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Cougar Point 1/6	1A
Date:	Thursday, September 30, 2010	Sheet 8 of 48

RTC Circuitry(RTC)



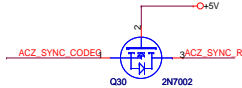
PCH2 (CLG)



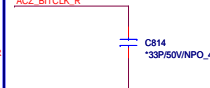
HDA Bus(CLG)



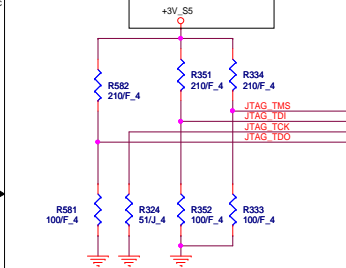
To Separate Codec Sync
by PD3



Reserve for RF



PCH JTAG Debug (CLG)

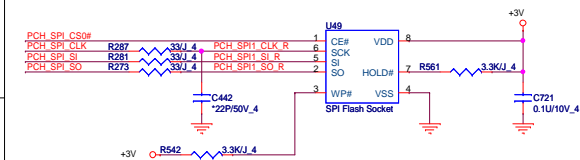


PCH Strap Table

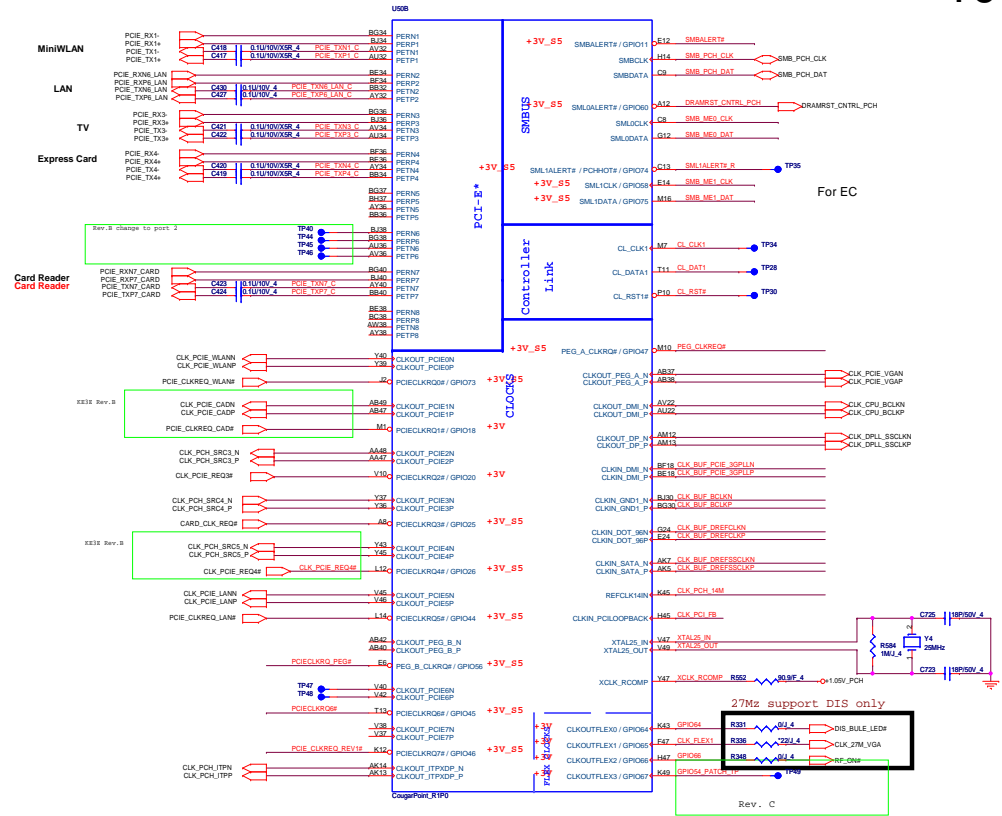
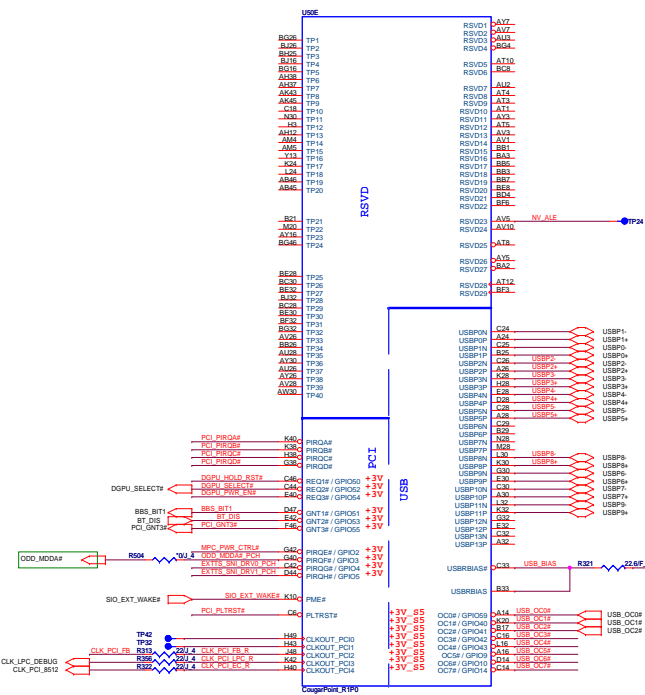
Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V_O - R307 - 1KJ_4 - SPCR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R608 - 1KJ_4 - PCI_GNT3#
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R592 - 330KJ_4 - PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]	R609 - 1KJ_4 - BBS_BIT1 R565 - 1KJ_4 - BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 - R590 - 1KJ_4 - ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R536 - 2.2KJ_4 - O+1.8V R538 - 1KJ_4 - DF_TVS H_SNB_IVB#
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R636 - 1KJ_4 - PLL_OVRV_EN
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R374 - 1KJ_4 - ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V_O - R282 - 1KJ_4 - PCH_SPI_SI
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

PCH Dual SPI (CLG)

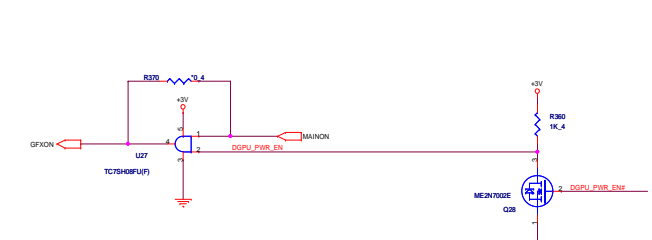
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00
Socket: DG008000031



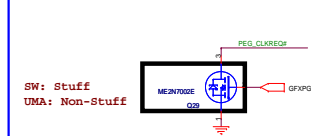
Cougar Point-M (PCI,USB,NVRAM)



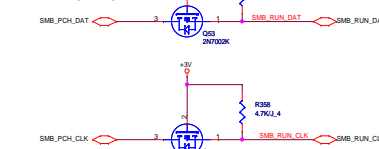
DGPU Power ON



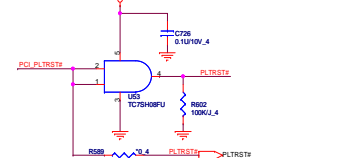
PEG CLK detect



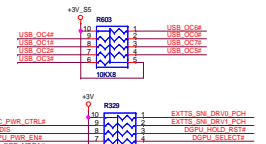
SMBus(CLK)



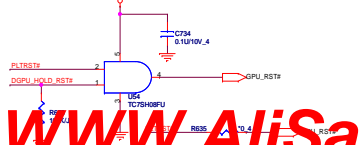
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



GPU RST#(CLG)

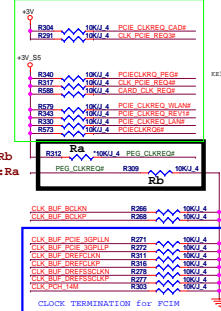


MPC Switch Control

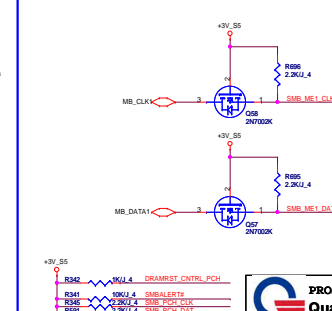
MPC_PWR_CTRL# Low = MPC ON
High = MPC OFF (Default)

MPC_PWR_CTRL# R330 10KΩ 4

CLK_REQ/Strap Pin(CLG)

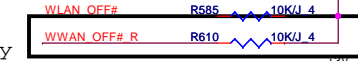
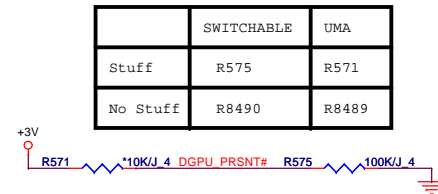
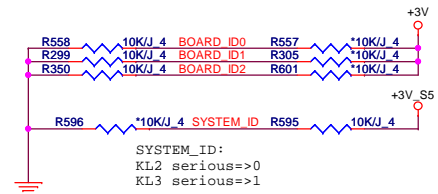
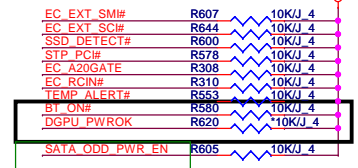


SMBus/Pull-up(CLG)

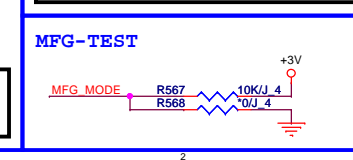
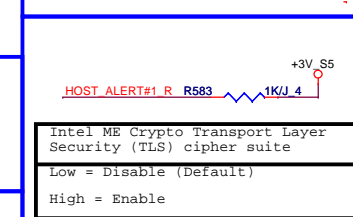
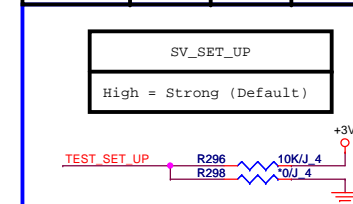


Cougar Point (GPIO,VSS_NCTF,RSVD)

GPIO Pull-up/Pull-down(CLG)

0526
Danny0526
Danny

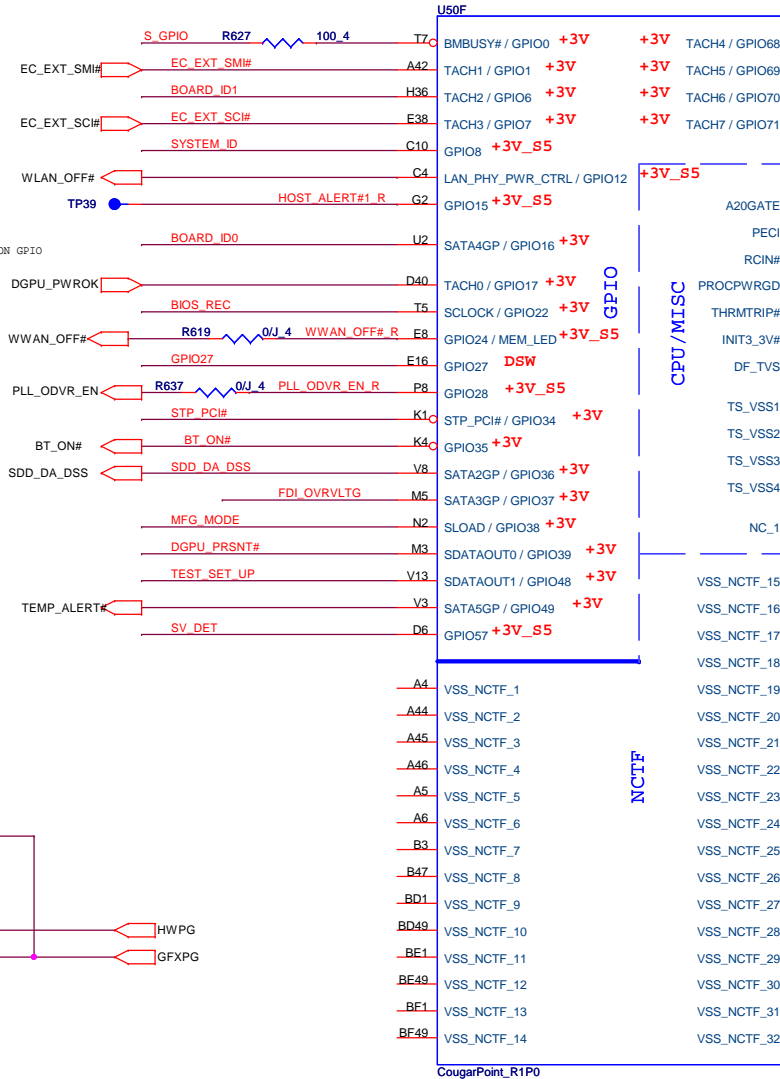
Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0



PROJECT : KL2D
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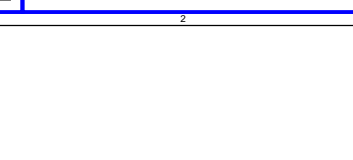
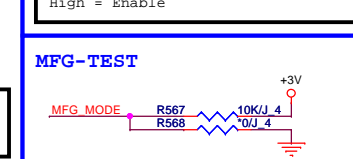
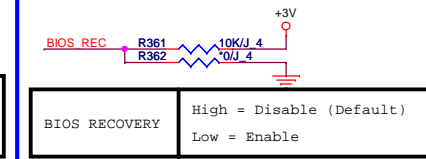
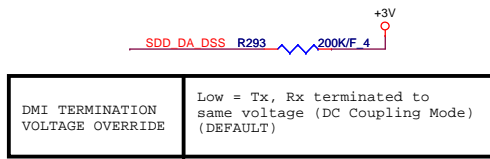
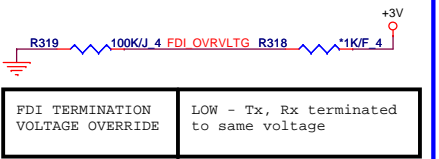
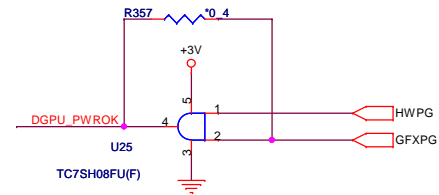
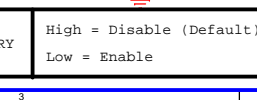
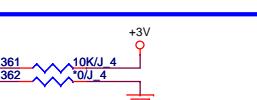
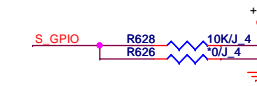
Size Document Number
Cougar Point 4/6
Date: Thursday, September 30, 2010 Sheet 11 of 48 Rev 1A

check VR_ON GPIO

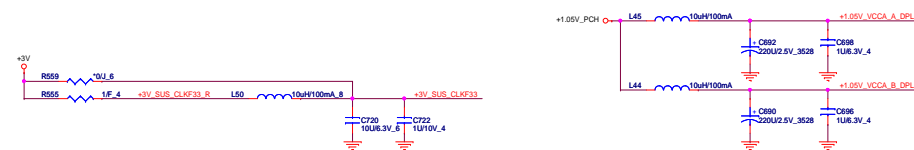
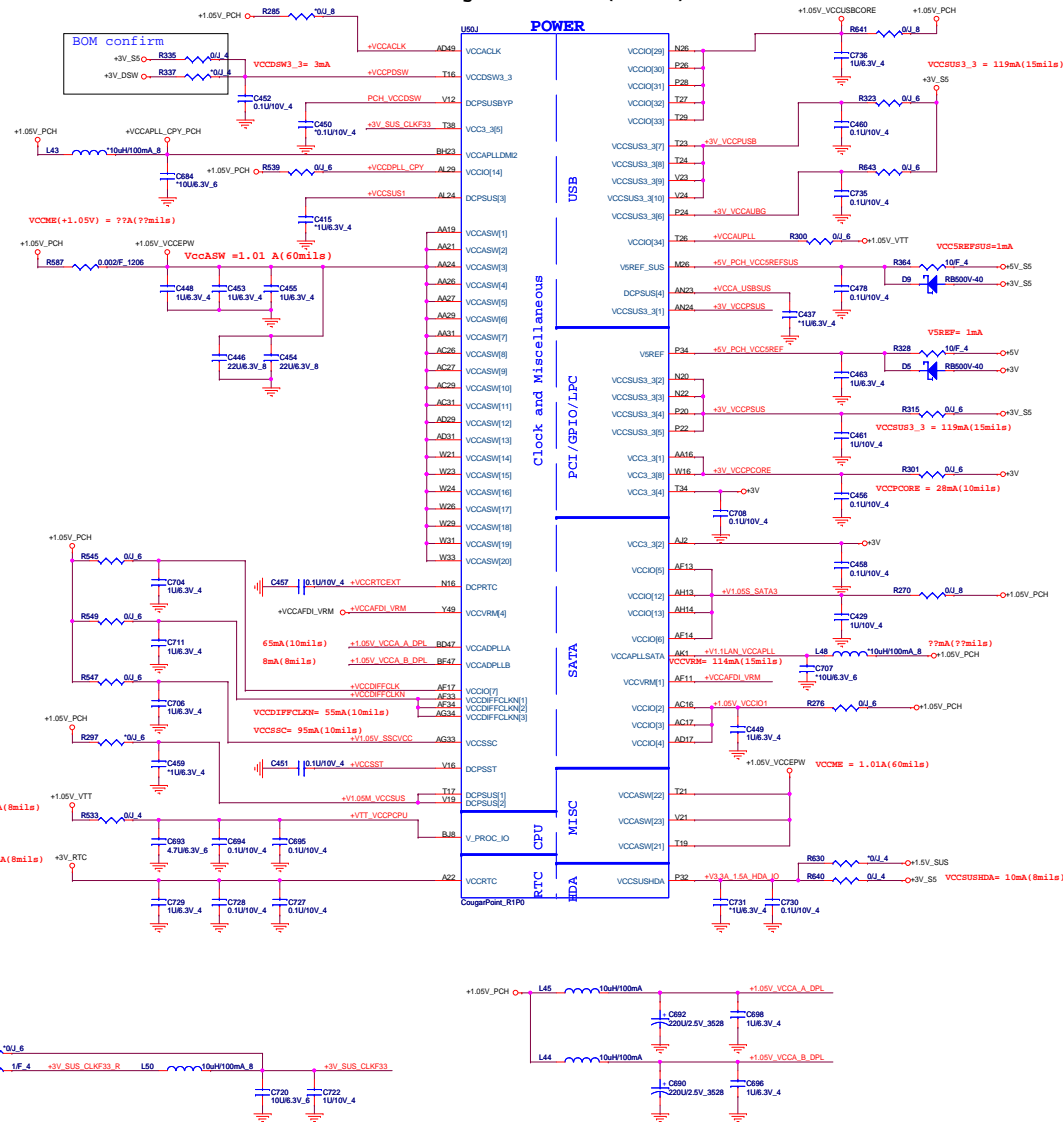


3/16 Connected to GND
DG rev0.9

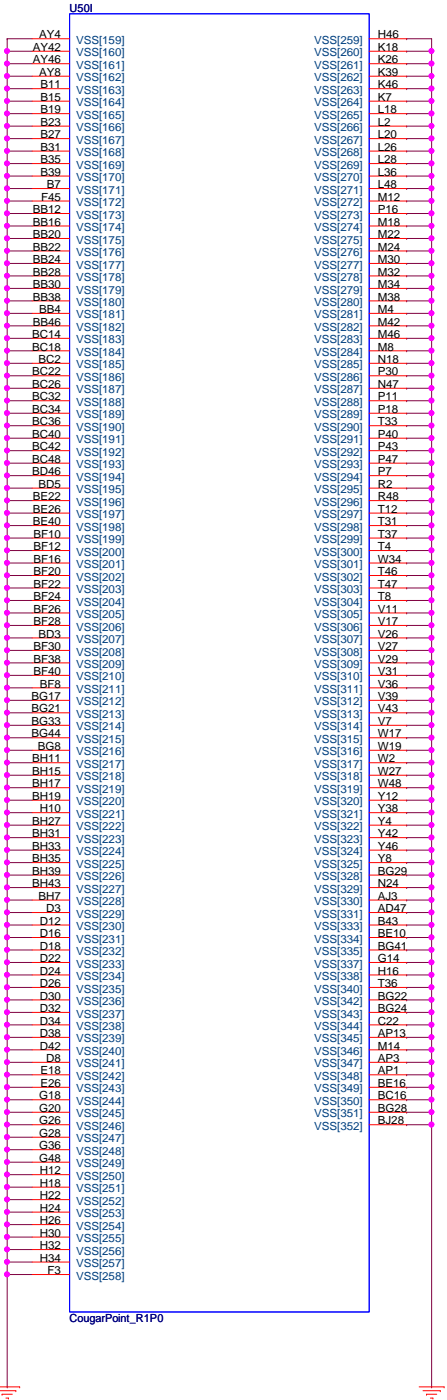
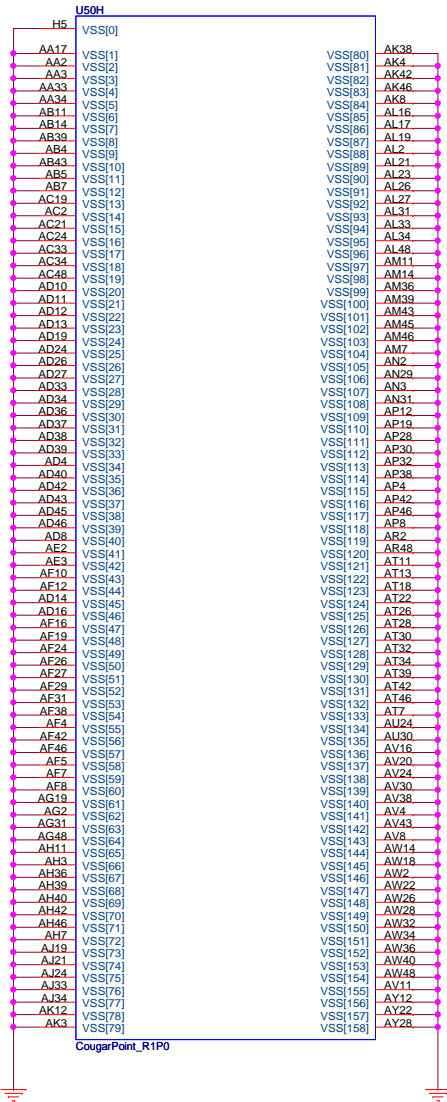
SGPIO



Cougar Point-M (POWER)

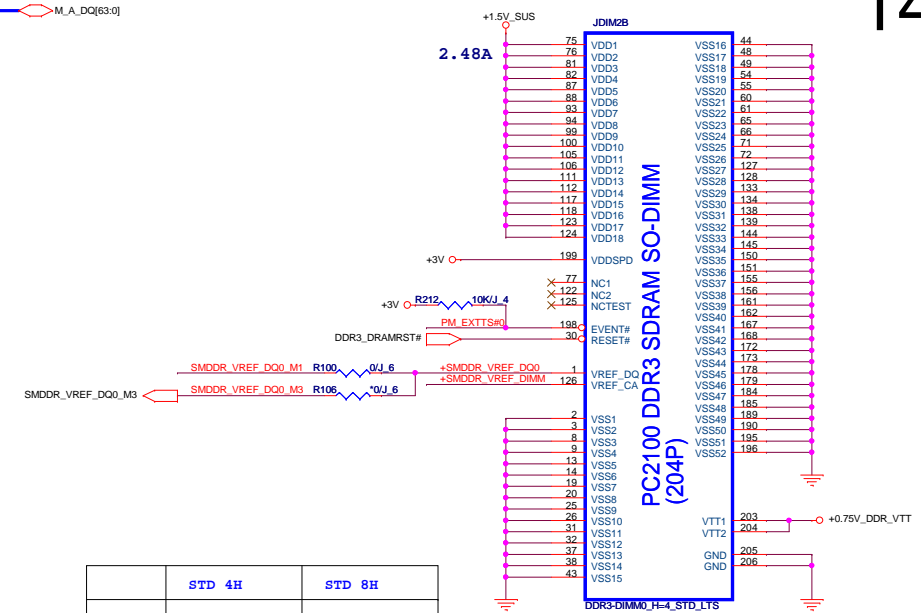
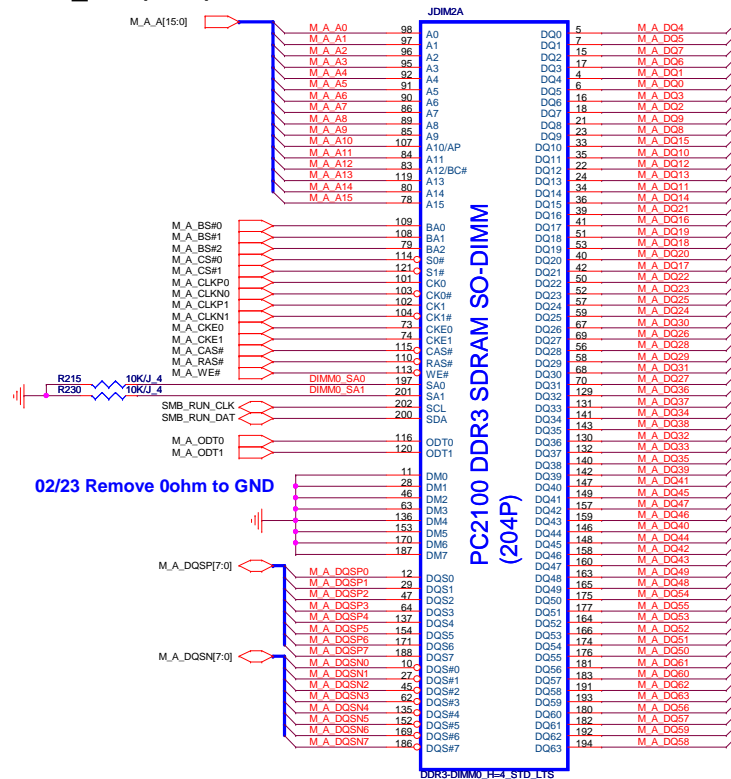


IBEX PEAK-M (GND)

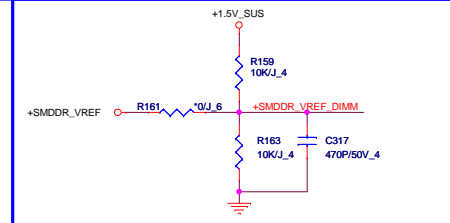
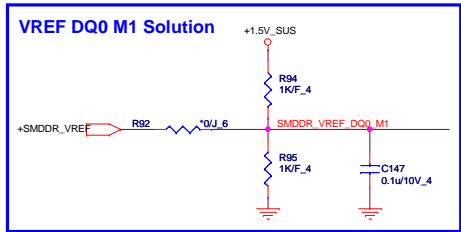
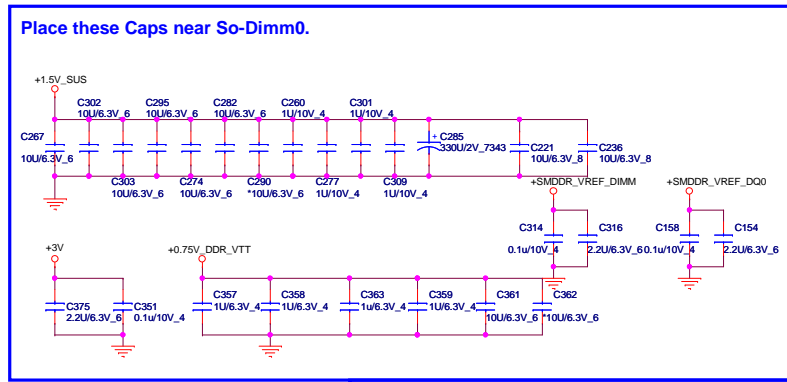


DDR_STD (DDR)

14

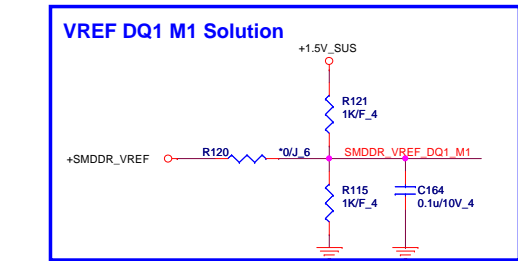
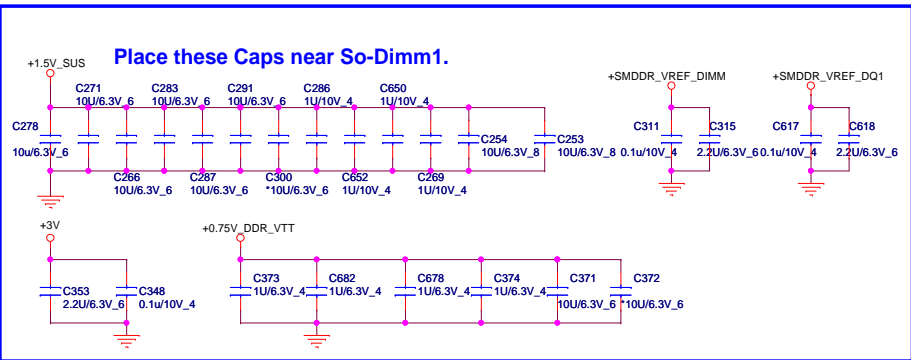
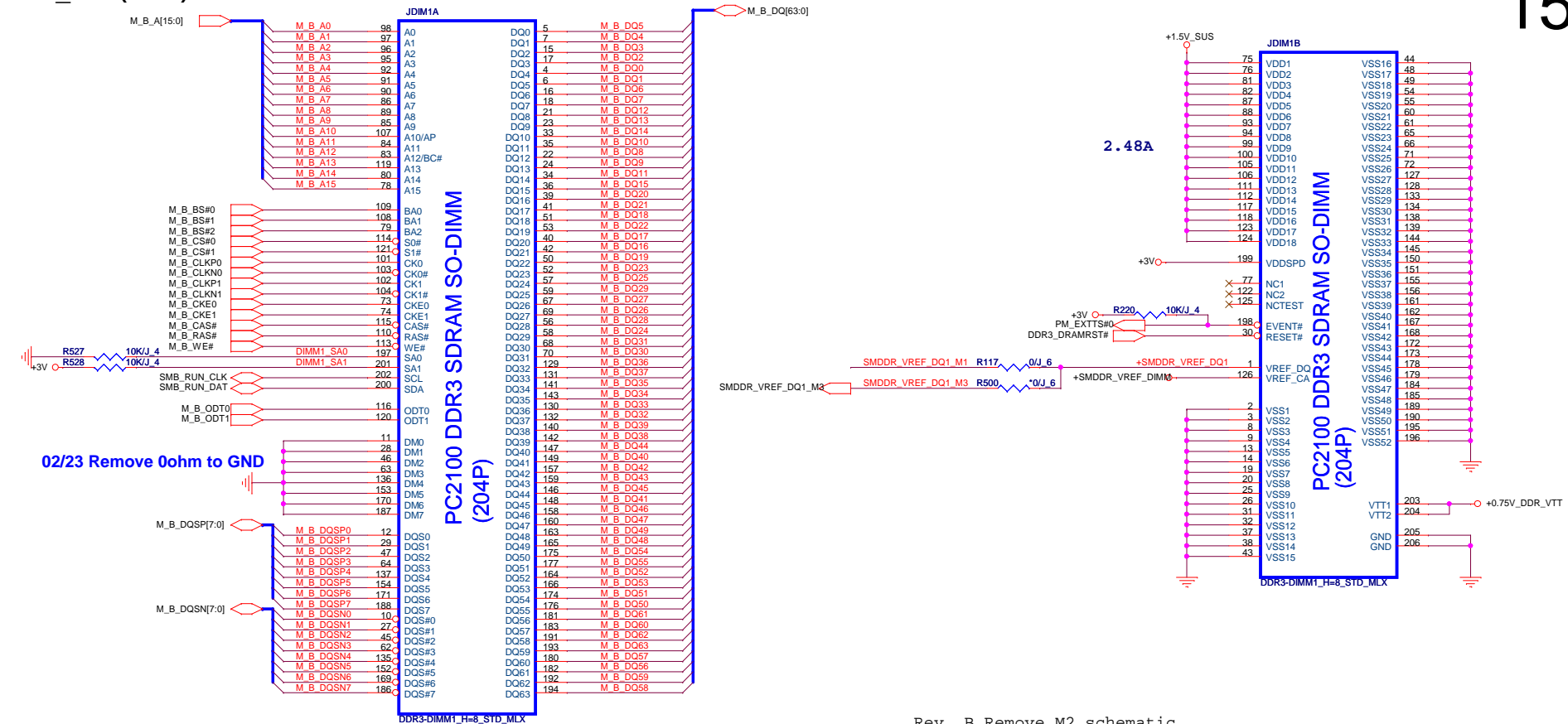


	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 4H type:DDR-C-2013289-204p		

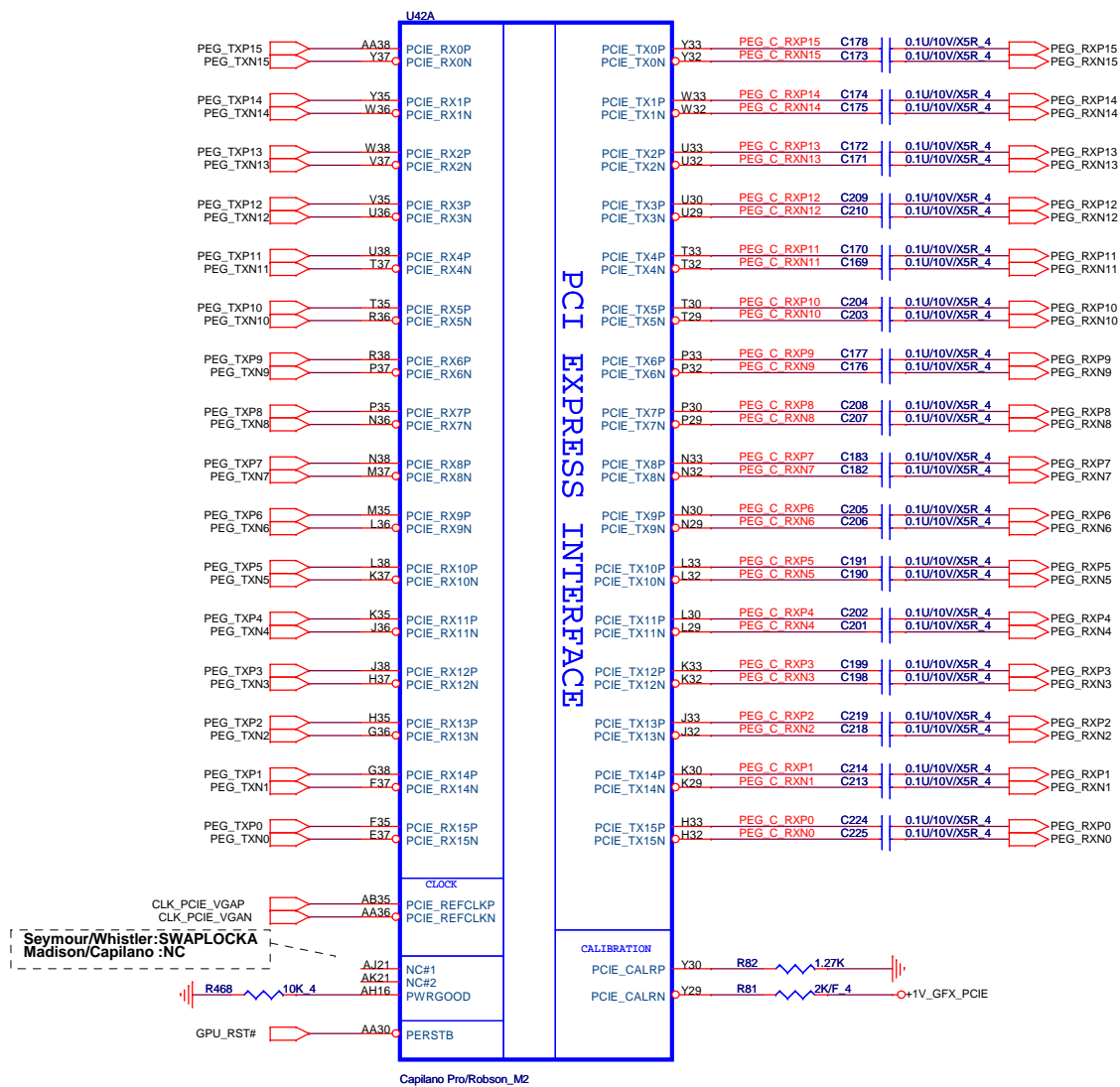


DDR_RVS (DDR)

15



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		



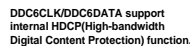
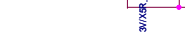
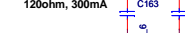
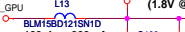
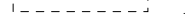
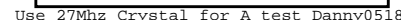
Note : Required Frequency = 800 MHz



Access to SCL and SDA
is mandatory on BAC0
design for debug
purposes.

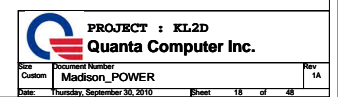


- 1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU PWROK

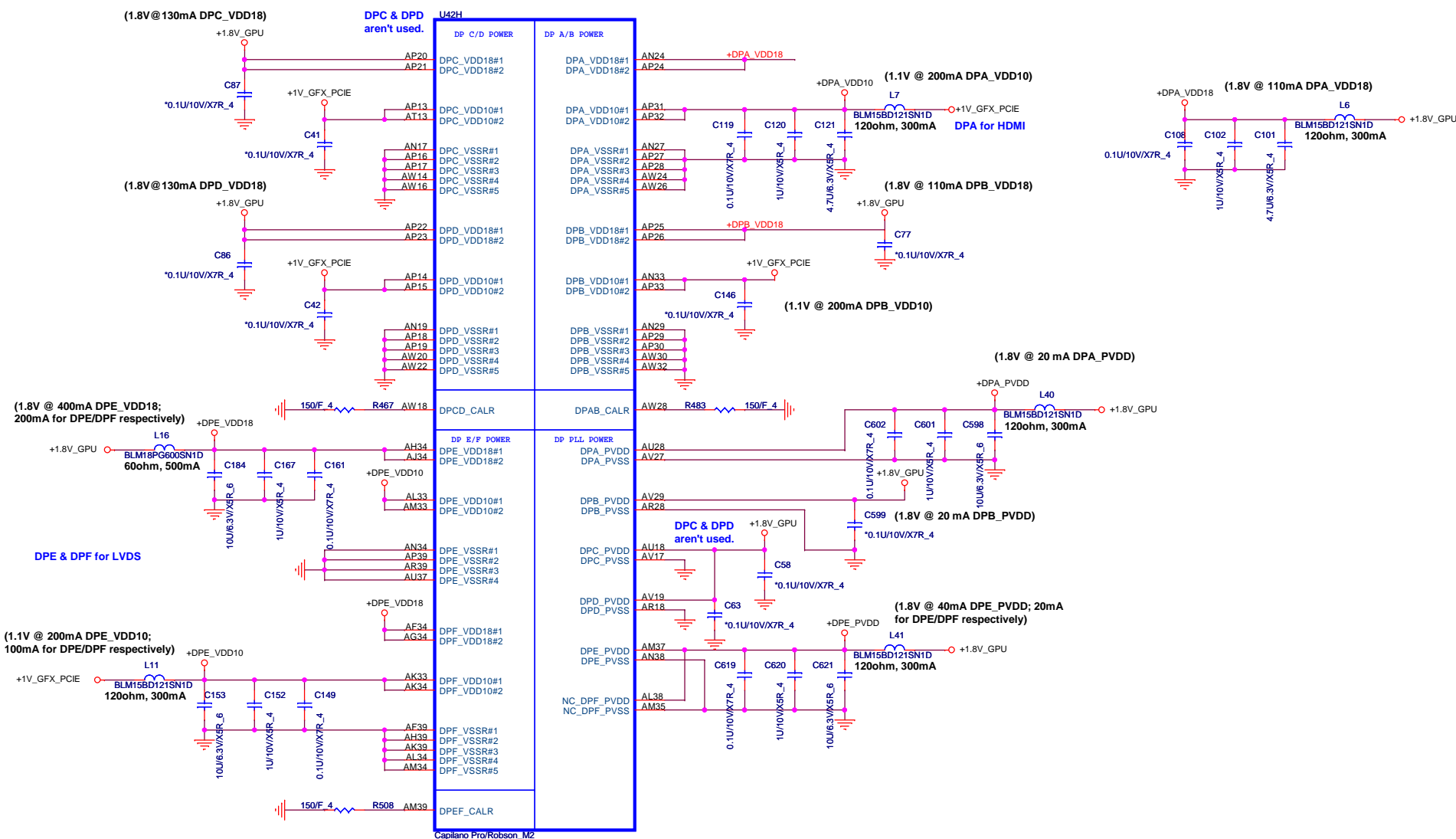


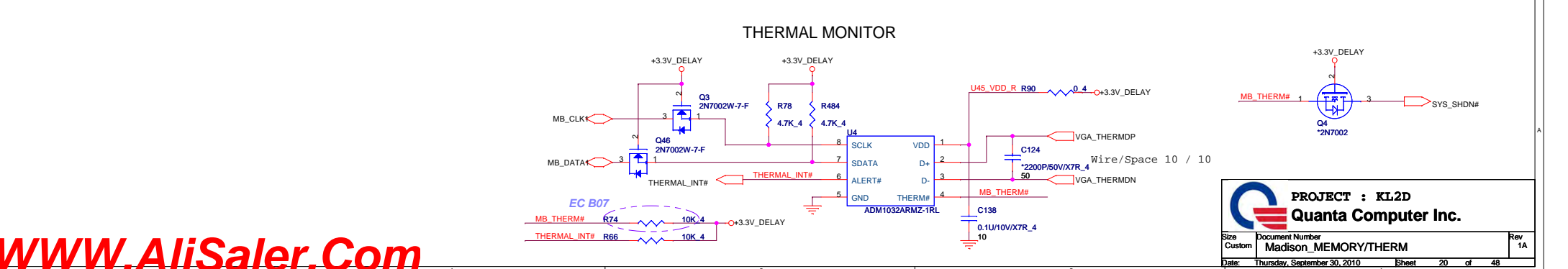
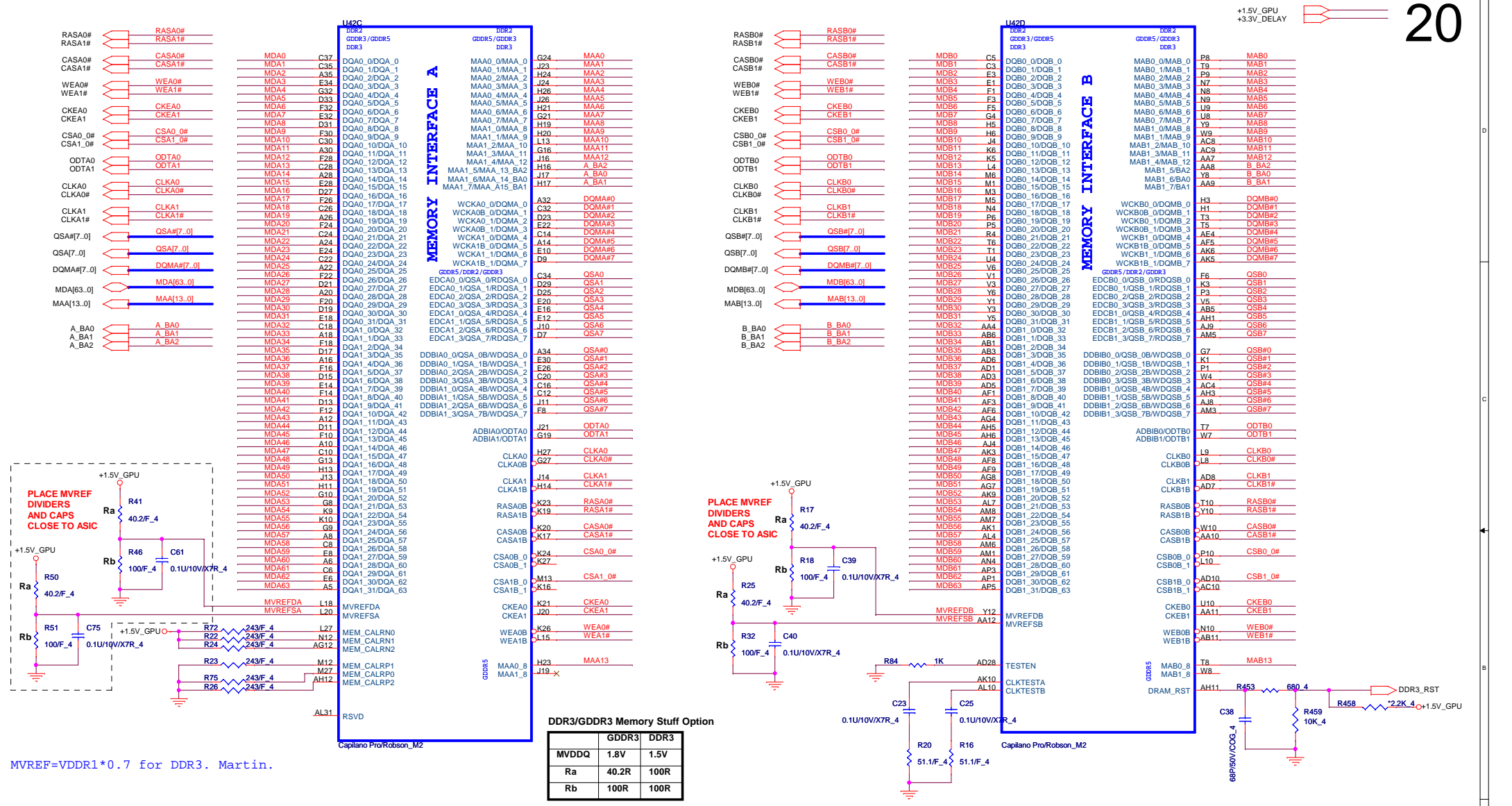
Layout Note:

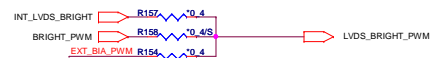




!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V

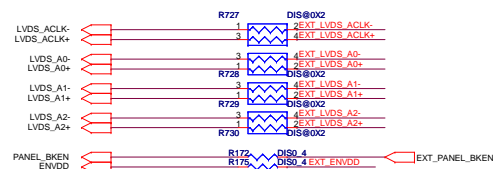




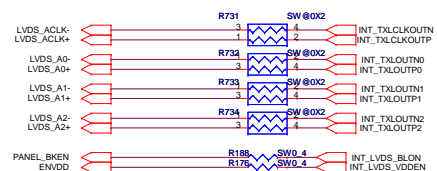


Remove MUX

Mount for DIS only



Mount for SW



CRT

Mount for DIS only



Mount for SW

Mount for DIS only

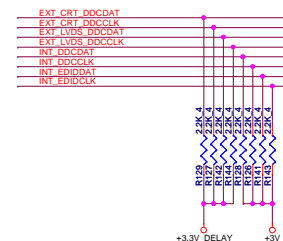


Mount for SW

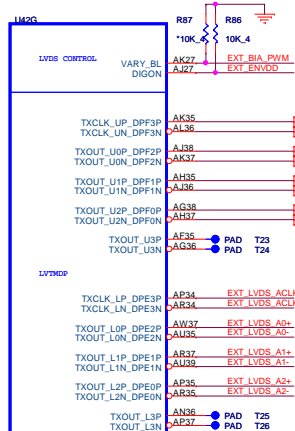
Mount for DIS only

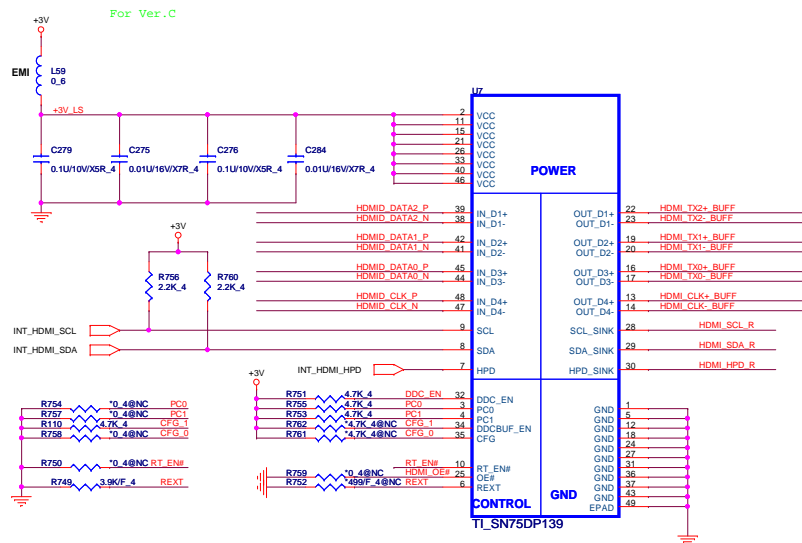


Mount for SW



Create new page for HDMI function....By Danny 0510

+5V
+3V
+3.3V_DELAY

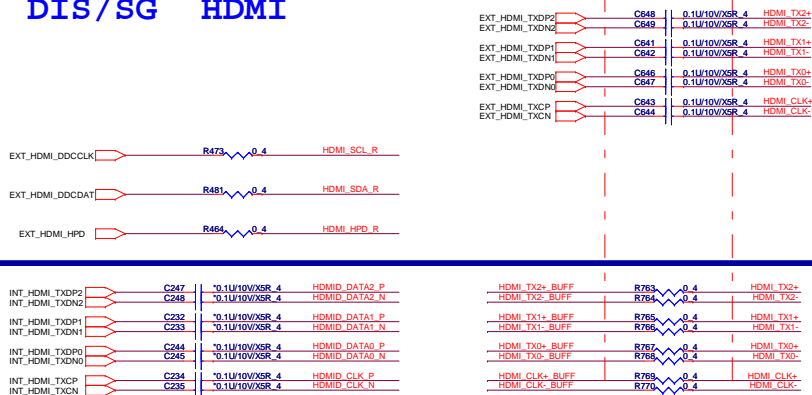


EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommended
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

PS8101 Pin34/35 is NC
SCL/SDA Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:-0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:-0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:-0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:-0.36V VOL:0.6V

For EMI request

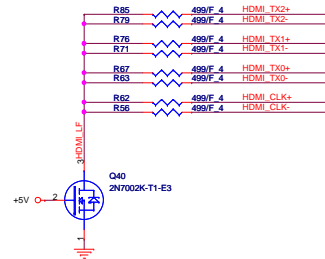
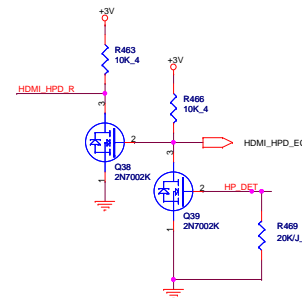
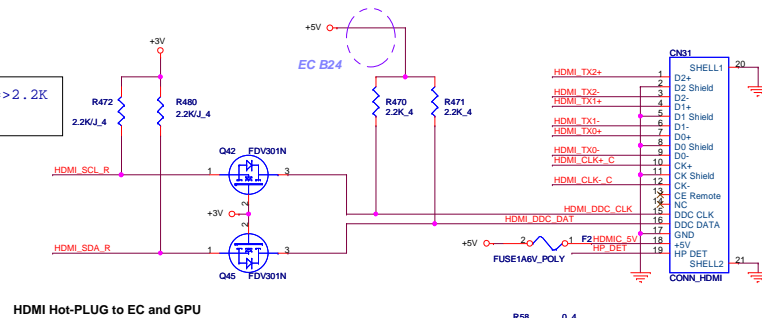
DIS/SG HDMI



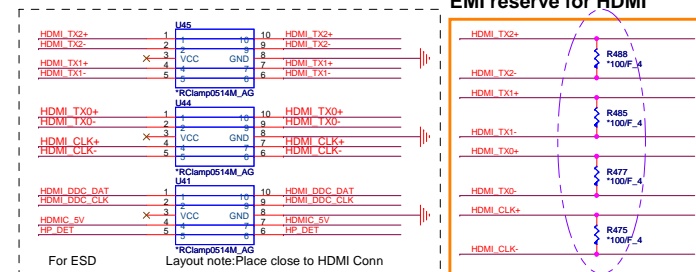
UMA Only HDMI

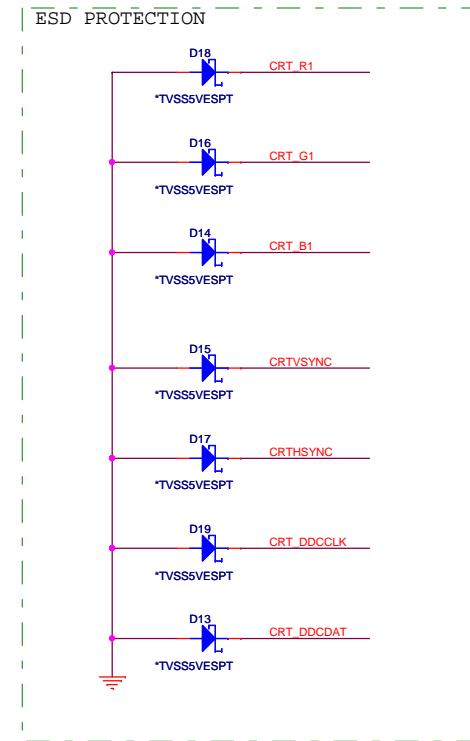
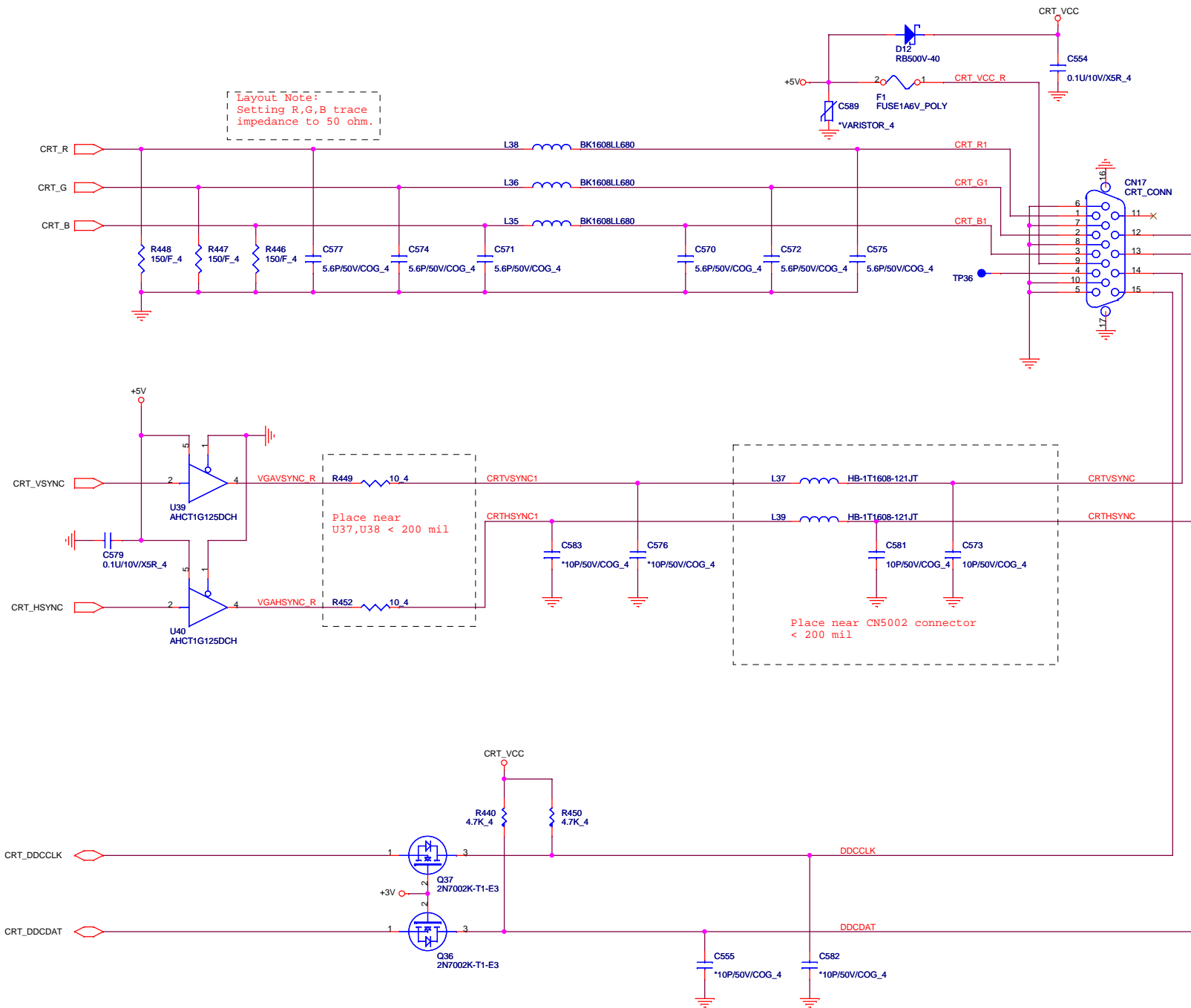
Co-lay with TOP/BOT placement.
No any trace length allow.

For Intel PCH request =>2.2K
ATI=>4.7K

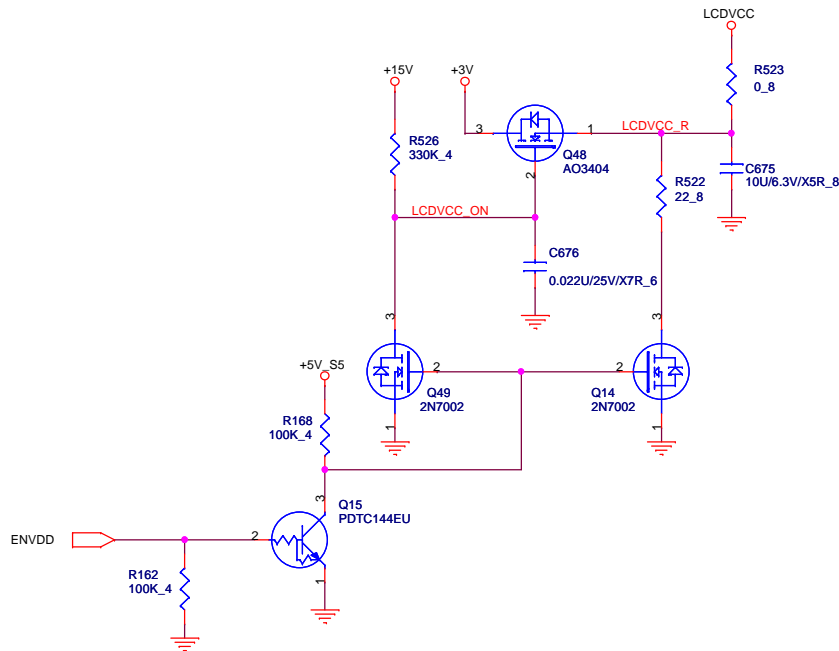


EMI reserve for HDMI

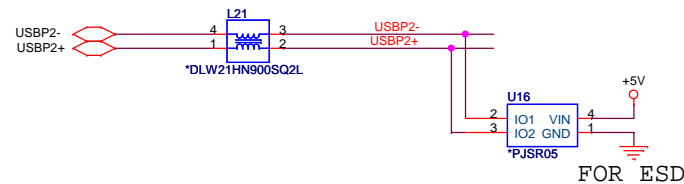
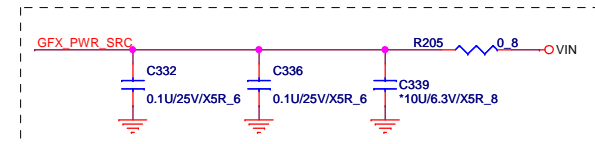
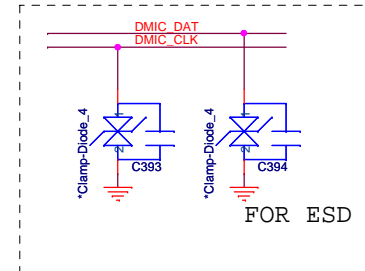
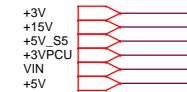
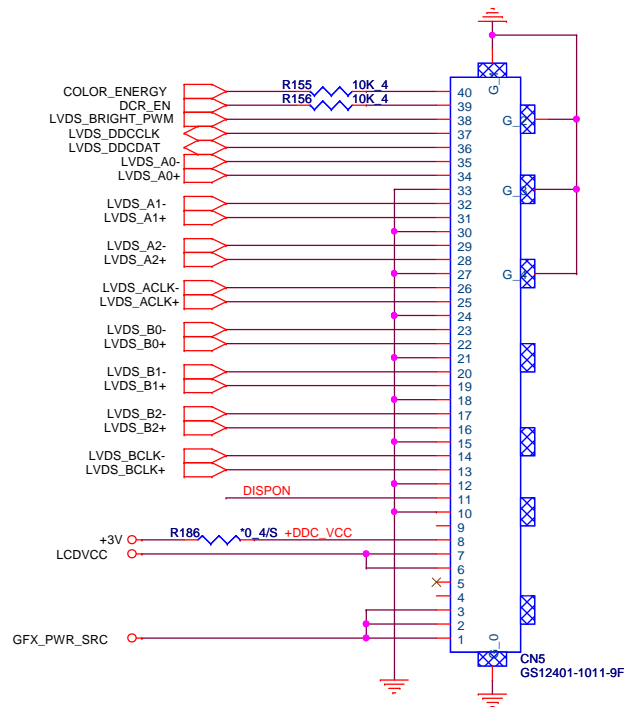
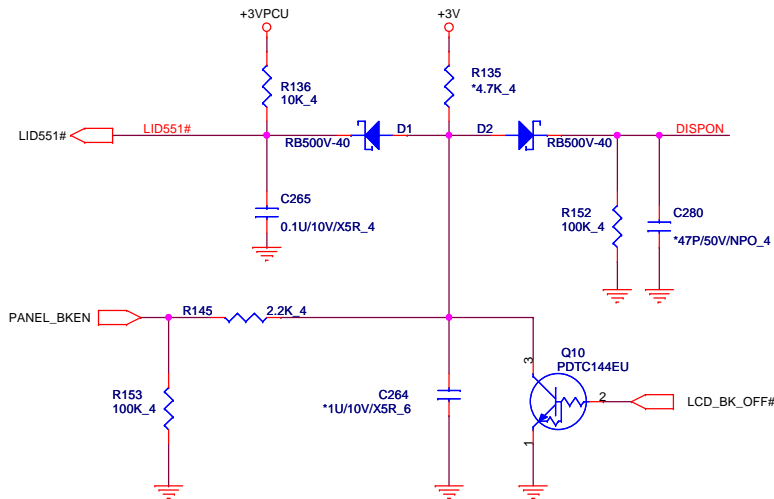




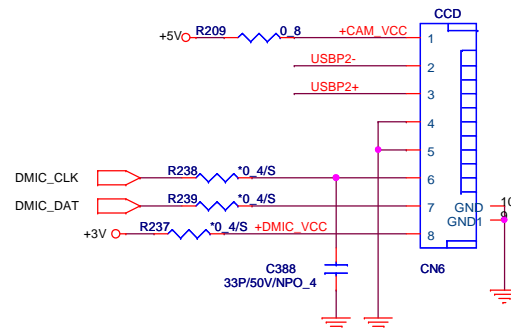
LCDVCC

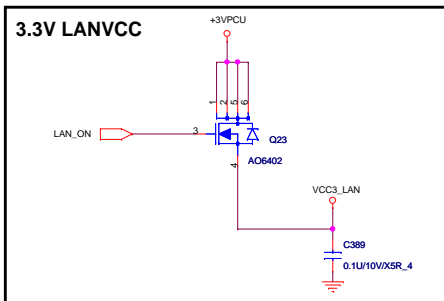
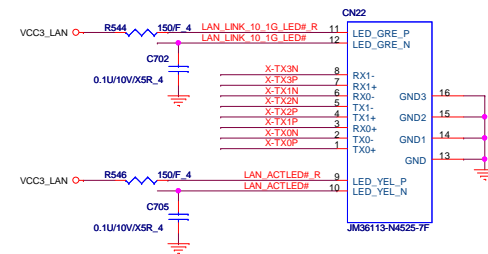


back light

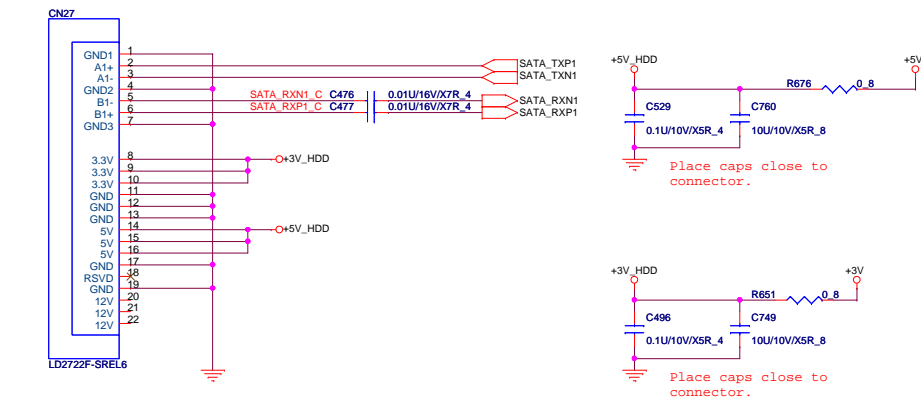


CAMERA

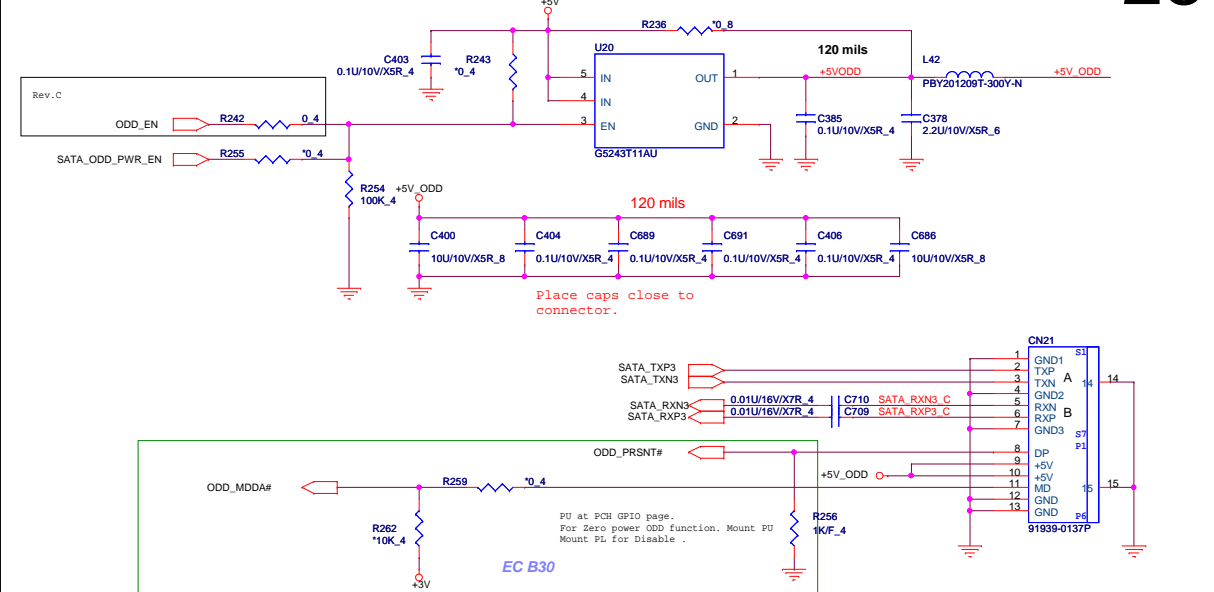




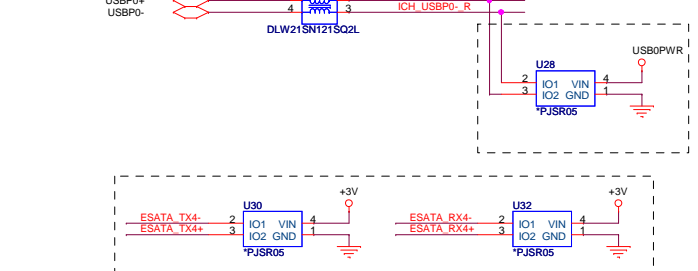
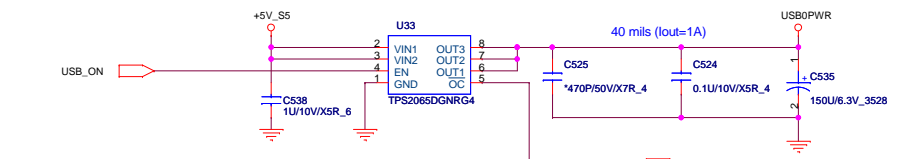
SATA HDD Connector.



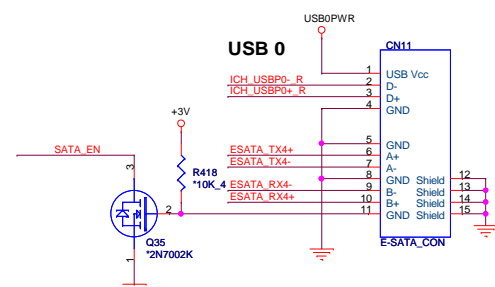
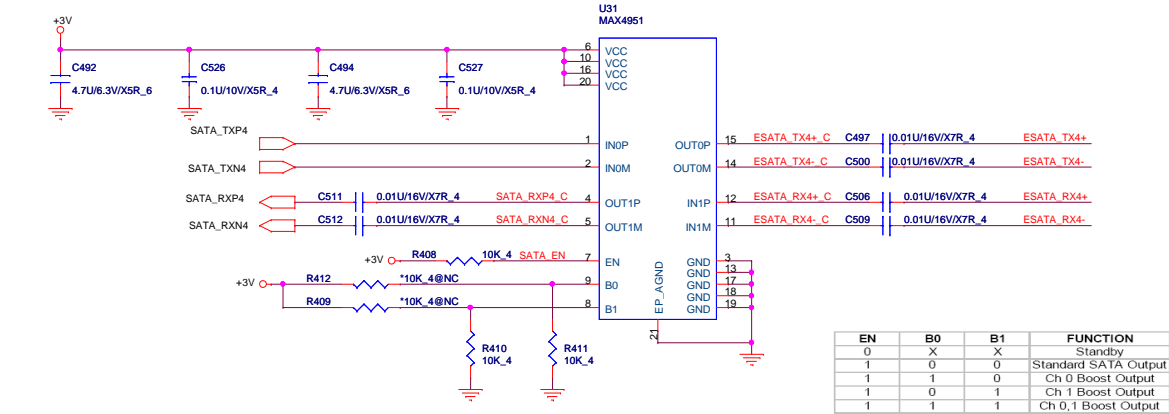
SATA ODD Connector.



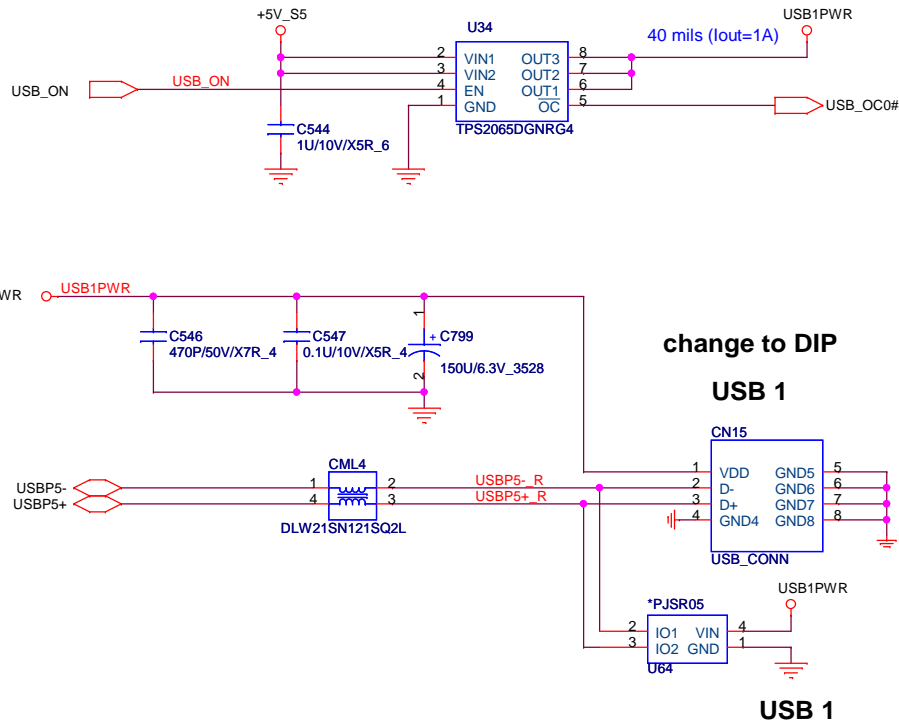
USB + E-SATA



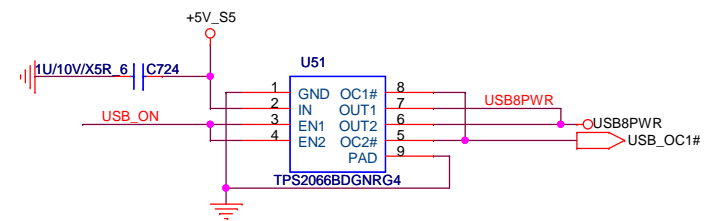
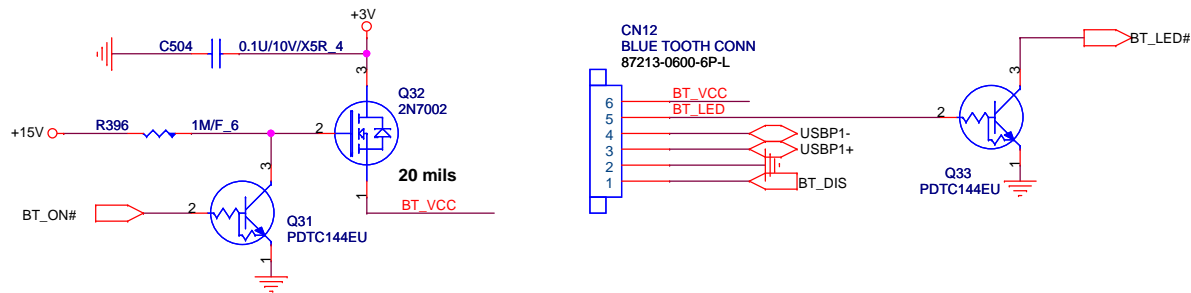
E-SATA RE-DRIVER

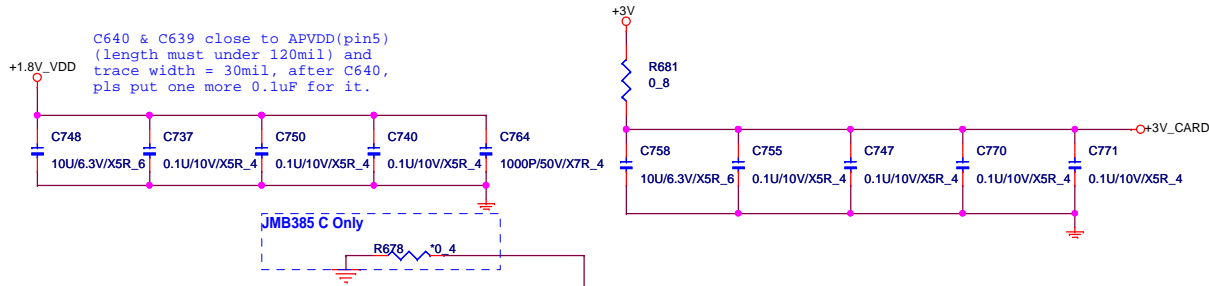


USBX3

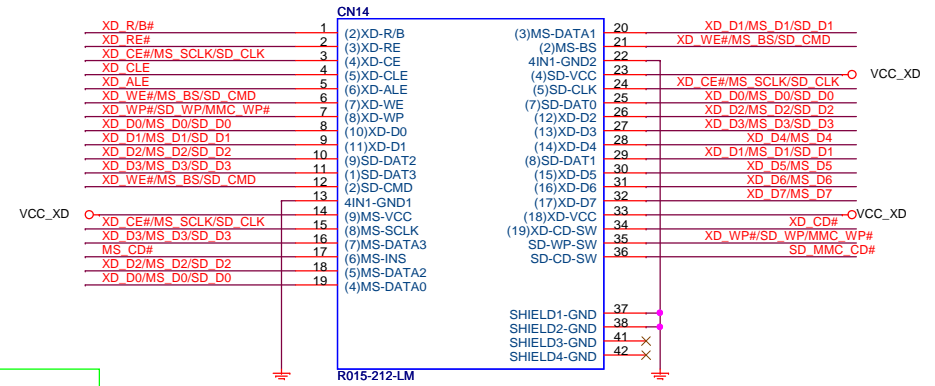


BLUETOOTH



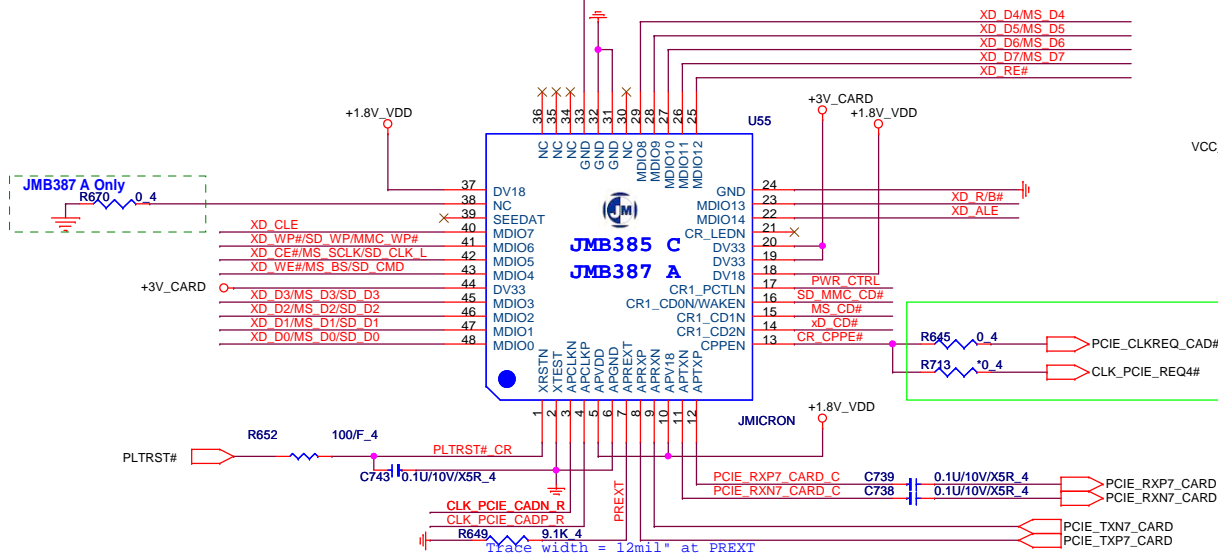
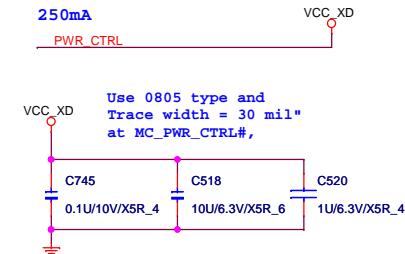


7 IN 1 CARD READER

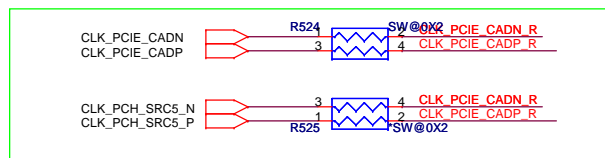


Rev. B

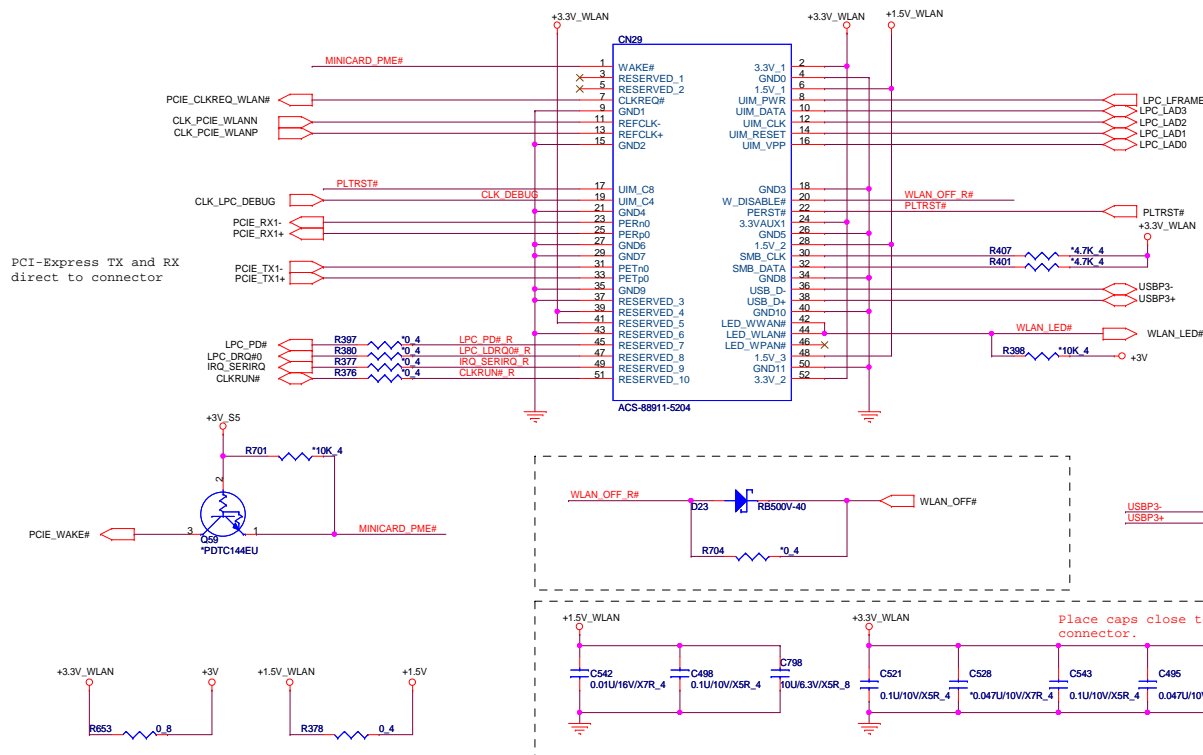
Memory Card Power Supply



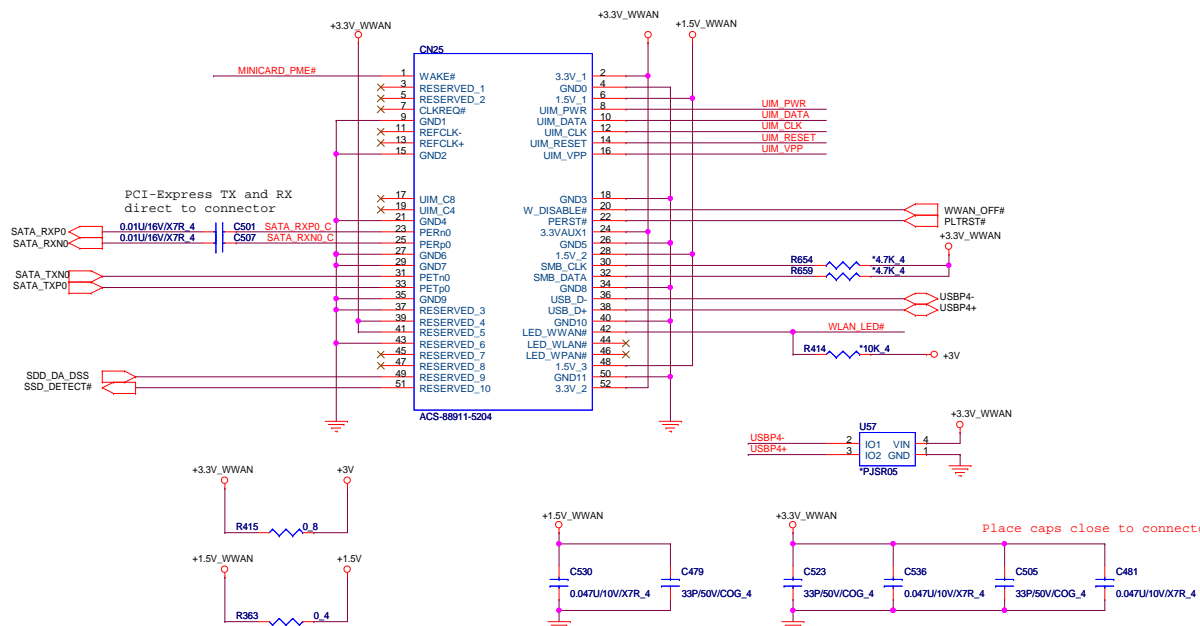
Rev. B



MiniCard WLA connector



MiniCard WWAN/SATA SSD connector

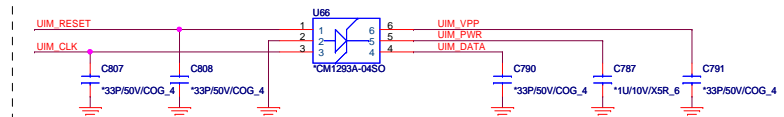


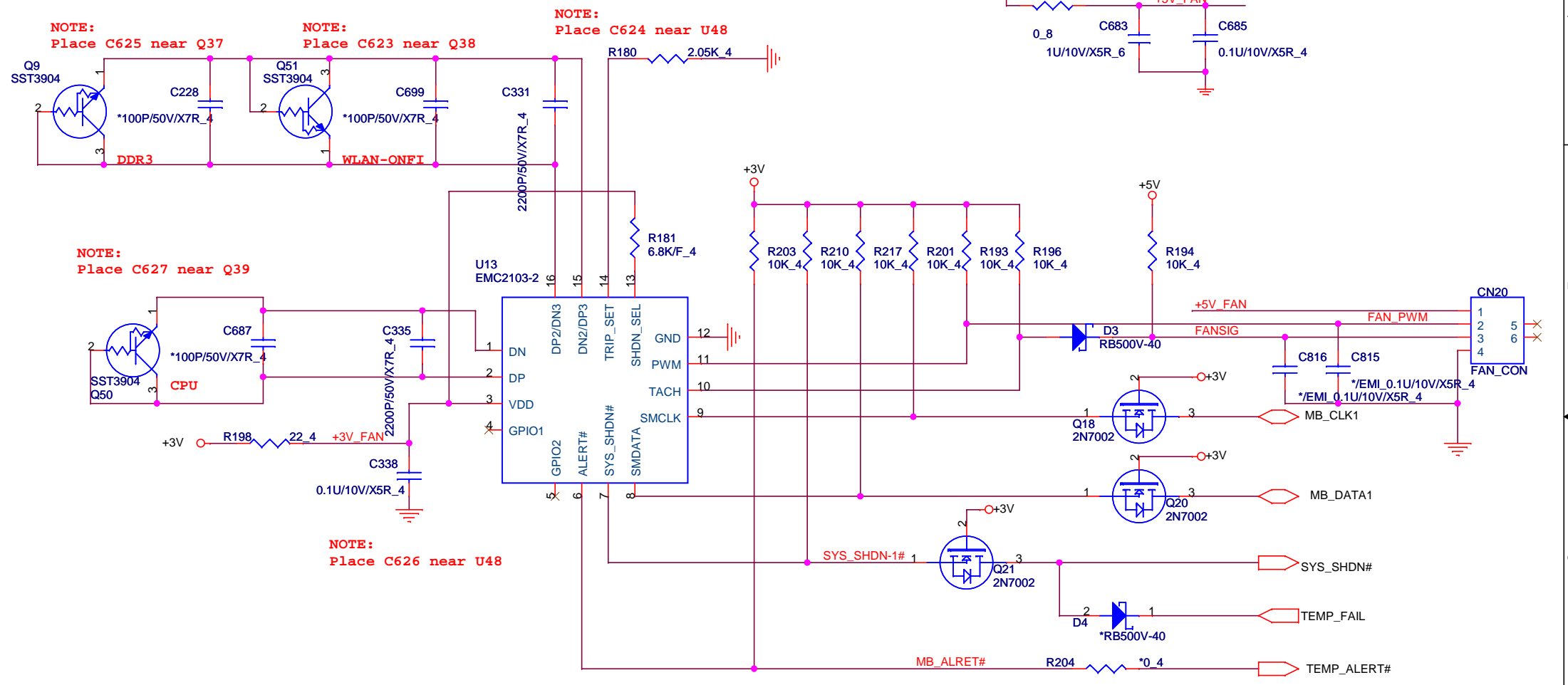
SIM Card CONN

SIM Card CONN

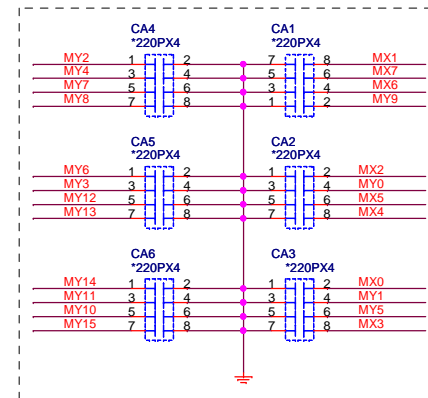
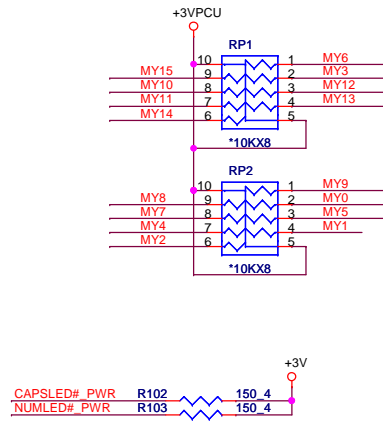
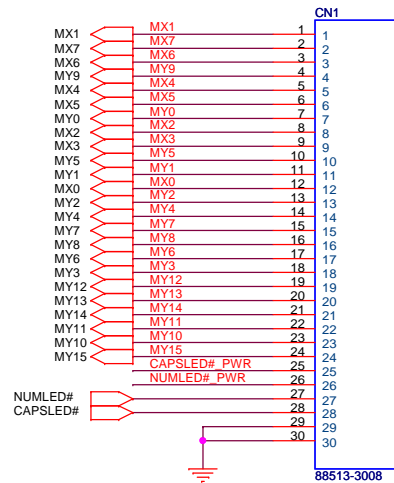
C.F modify 07.21

Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

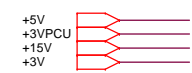




KEYBOARD

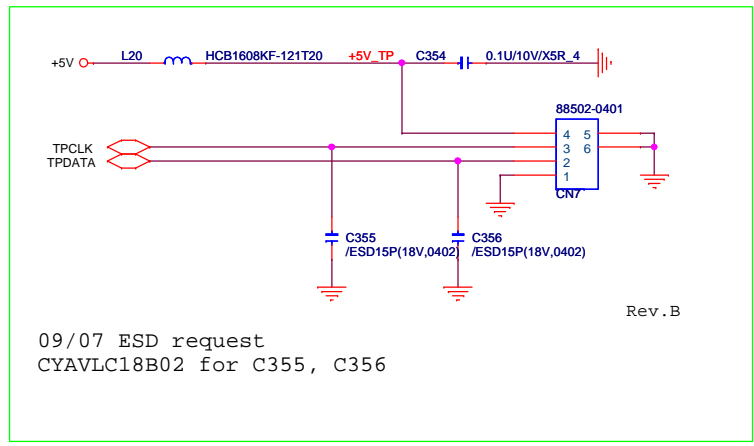


For EMI request



34

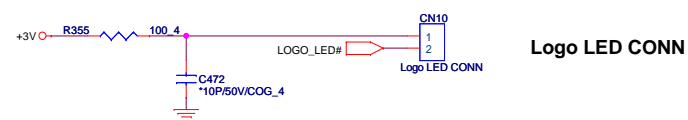
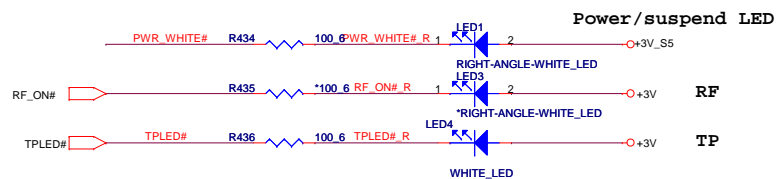
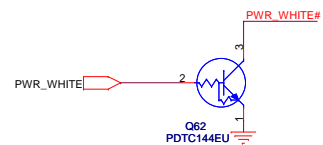
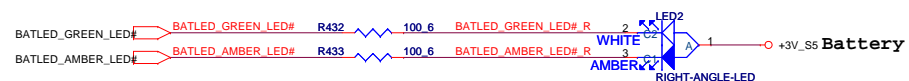
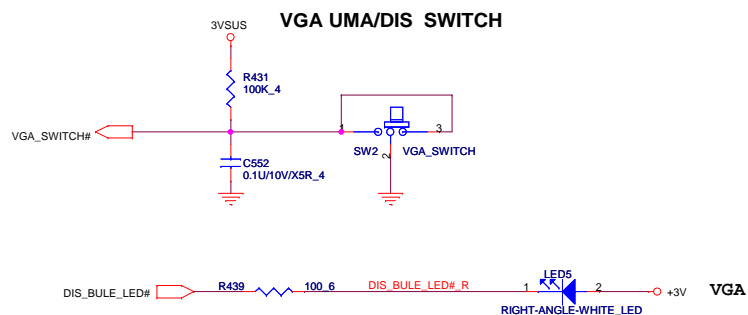
Touch pad



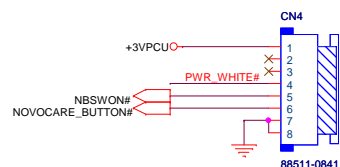
Backlight Keybaord Con.

Remove KB LED Schematic
Danny0513

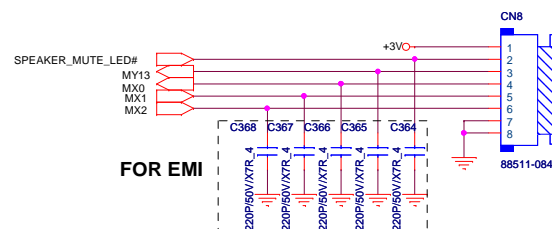
VGA UMA/DIS SWITCH



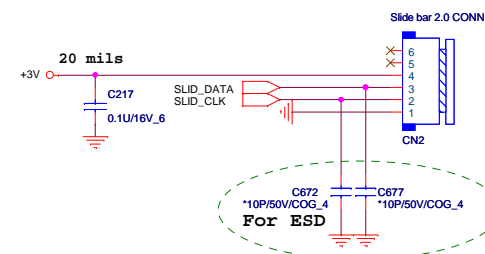
LEFT POWER BOARD



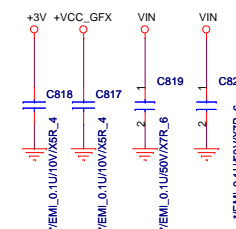
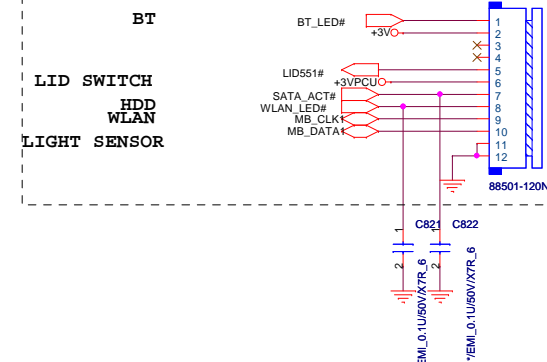
RIGHT VOLUME BOARD



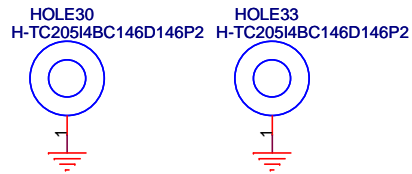
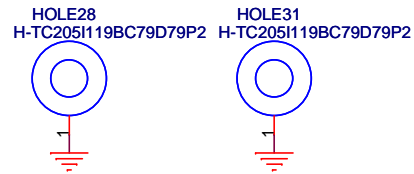
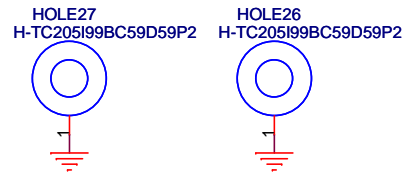
Slide bar 2.0



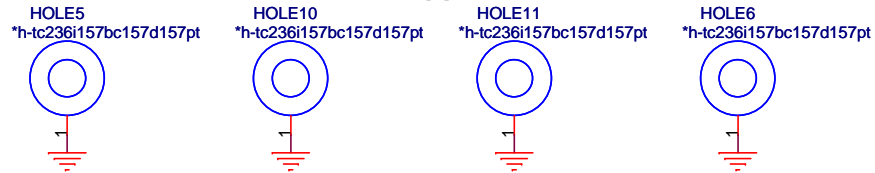
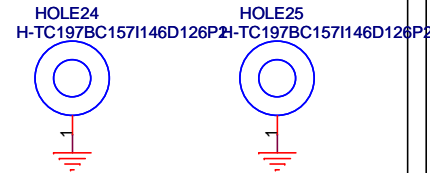
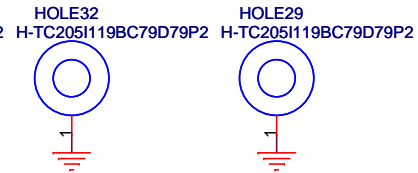
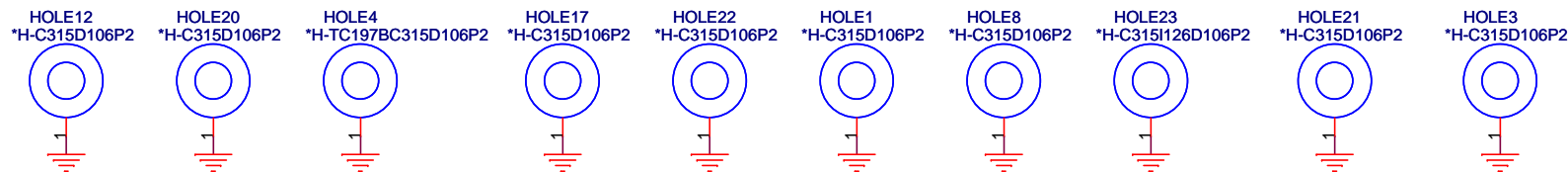
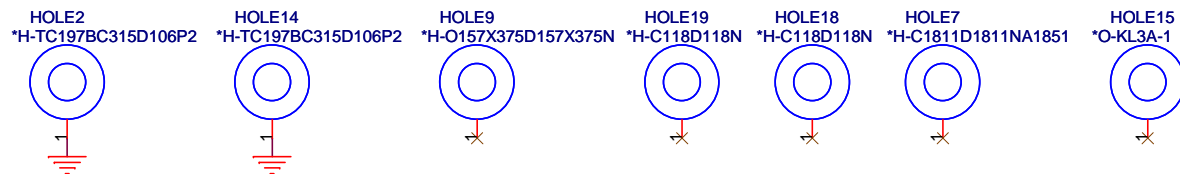
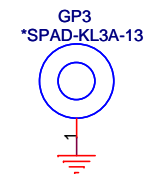
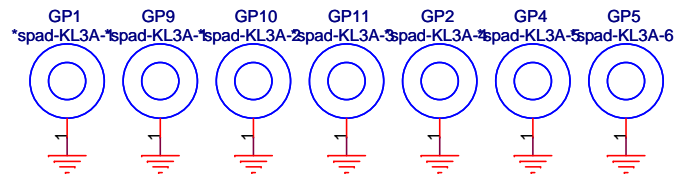
UP LED BOARD




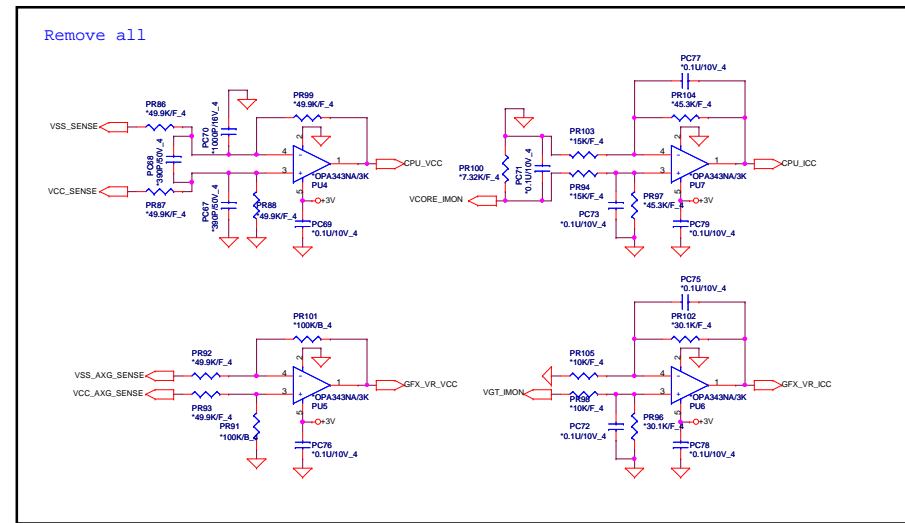
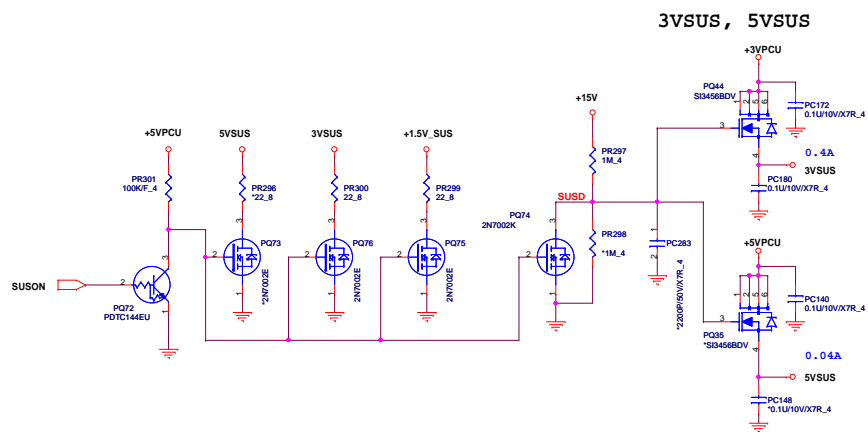
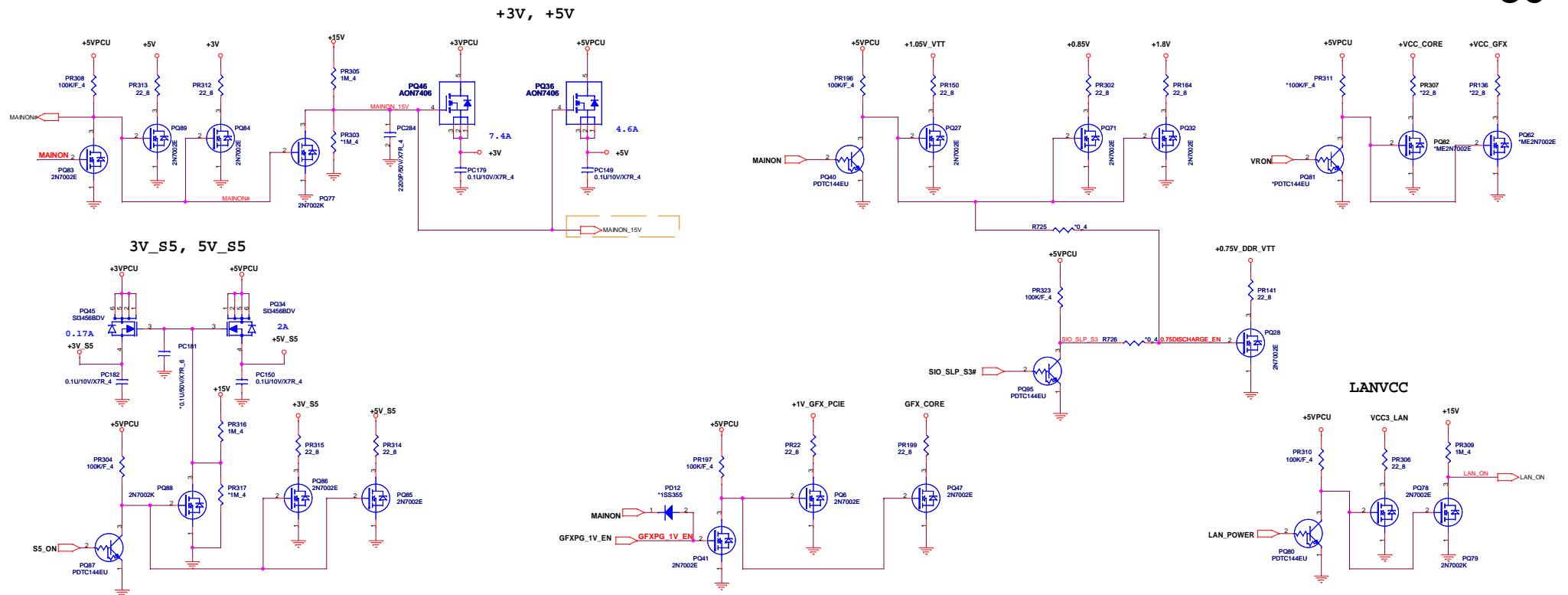


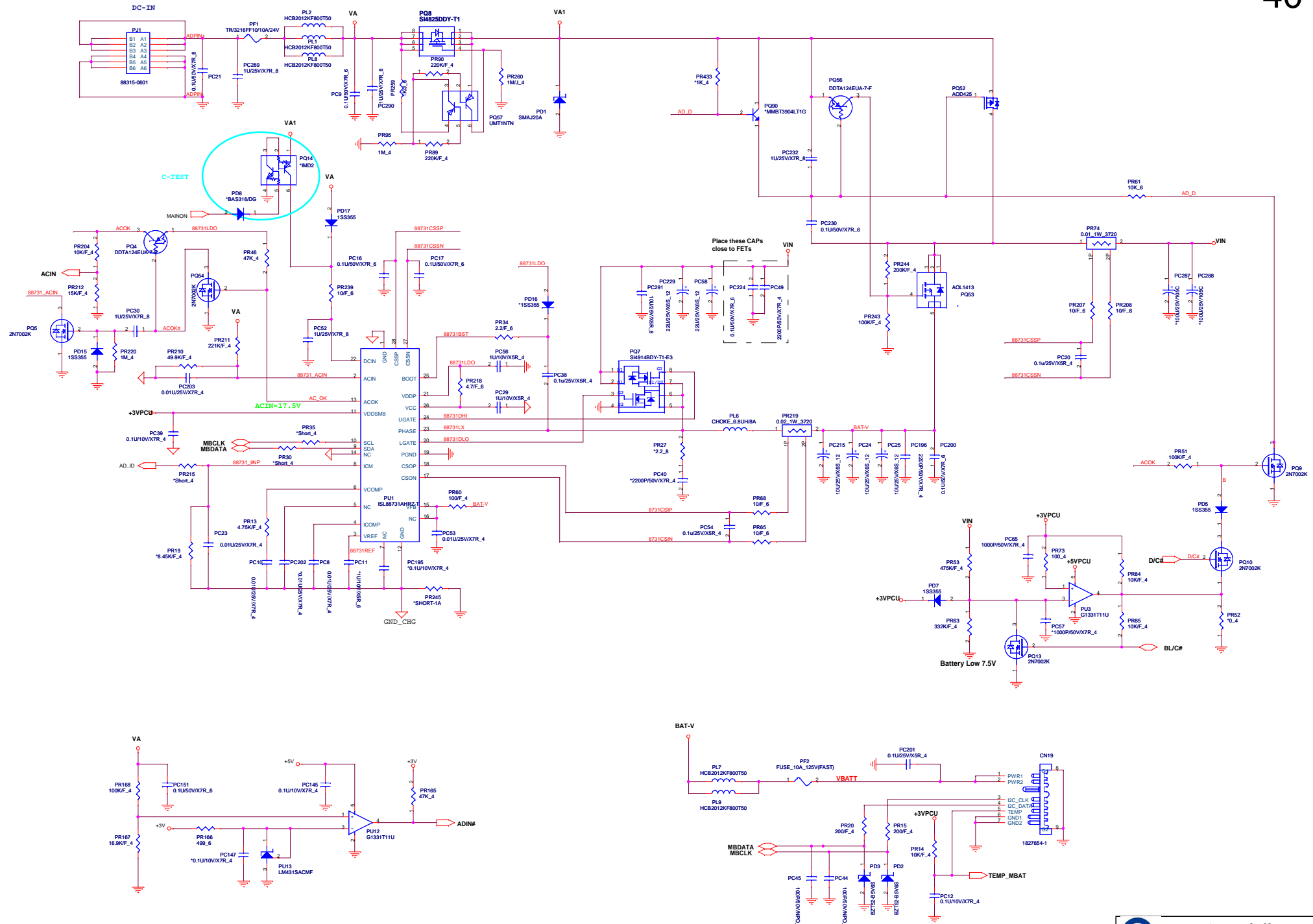
MiniCard WLAN**MiniCard WWAN****Hole for PCH support****Drink Hole****ESD for ESATA**

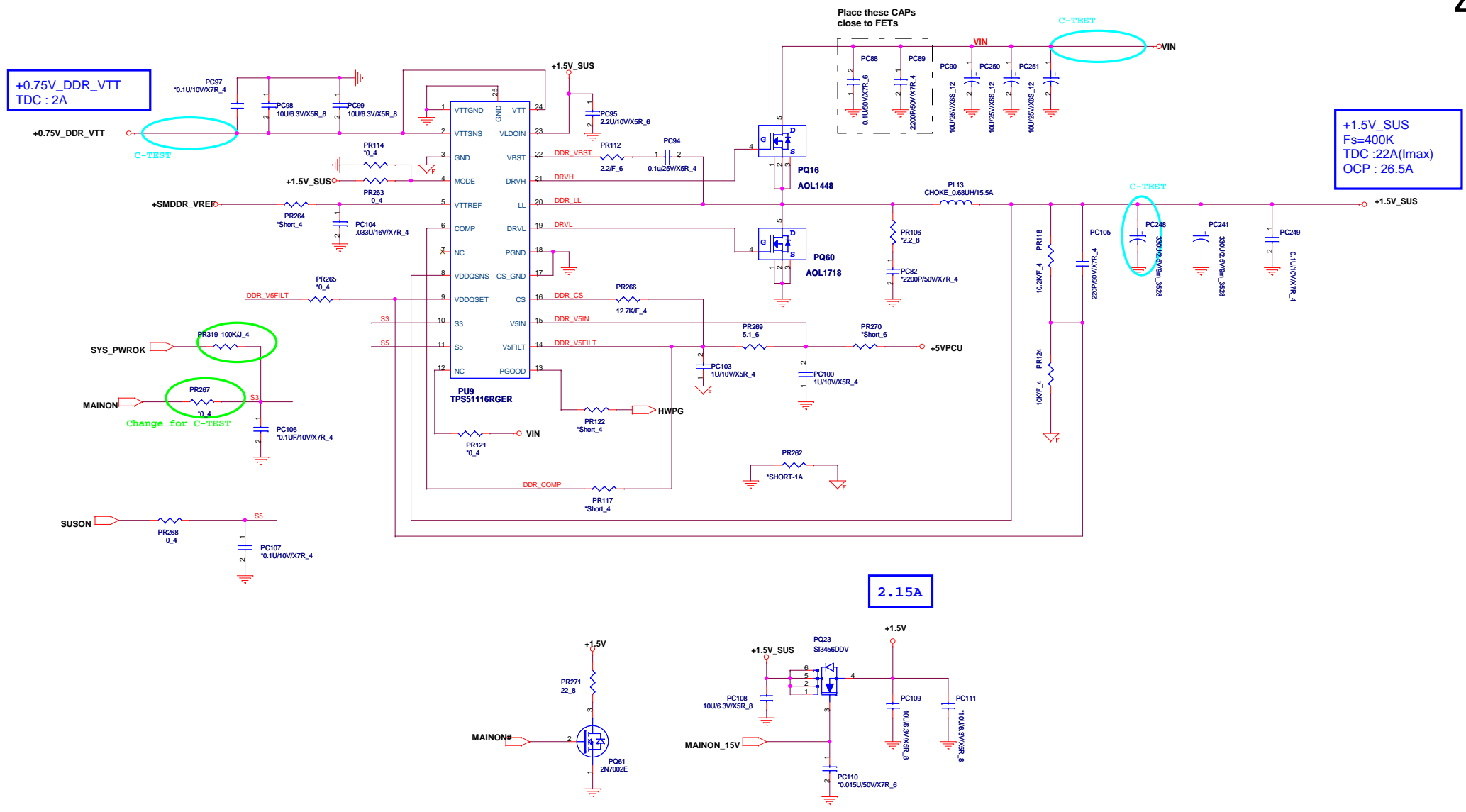
38

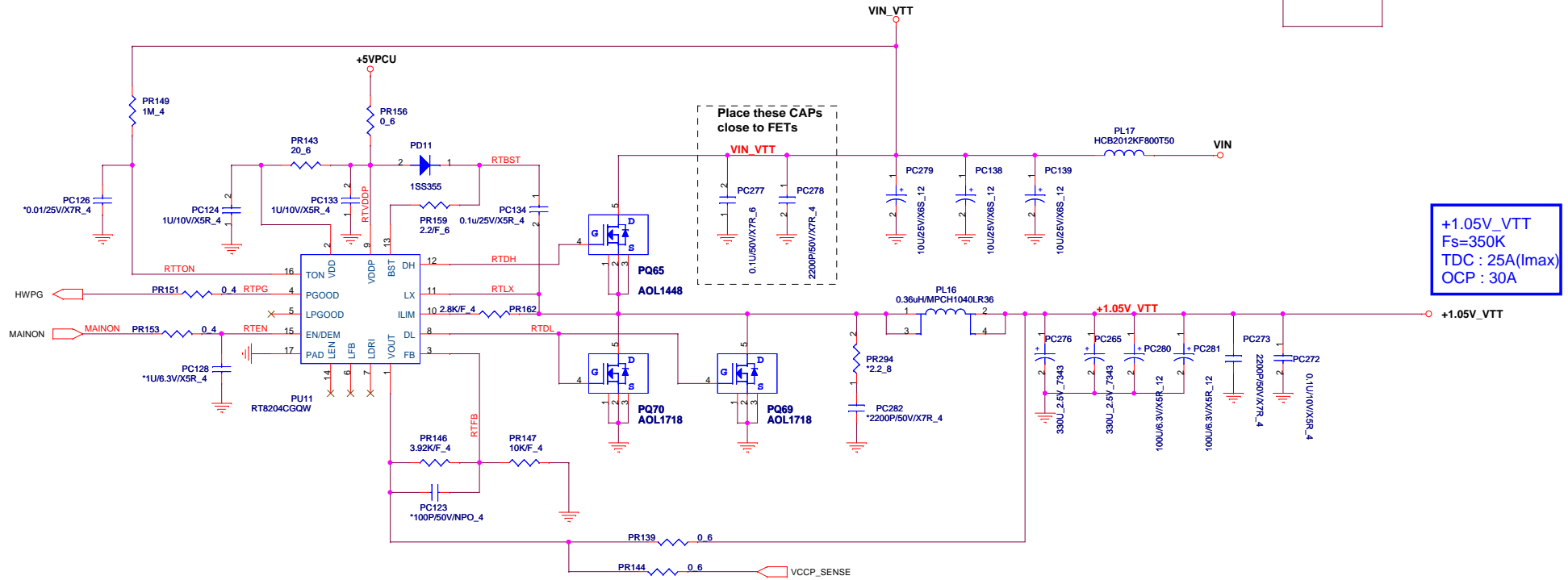
Hole for CPU support**VGA nut****MiniCard TV****Boundary Hole****Boundary Hole****Break Hole****Boundary Hole (ODD)****HDD PAD****ESD PAD**

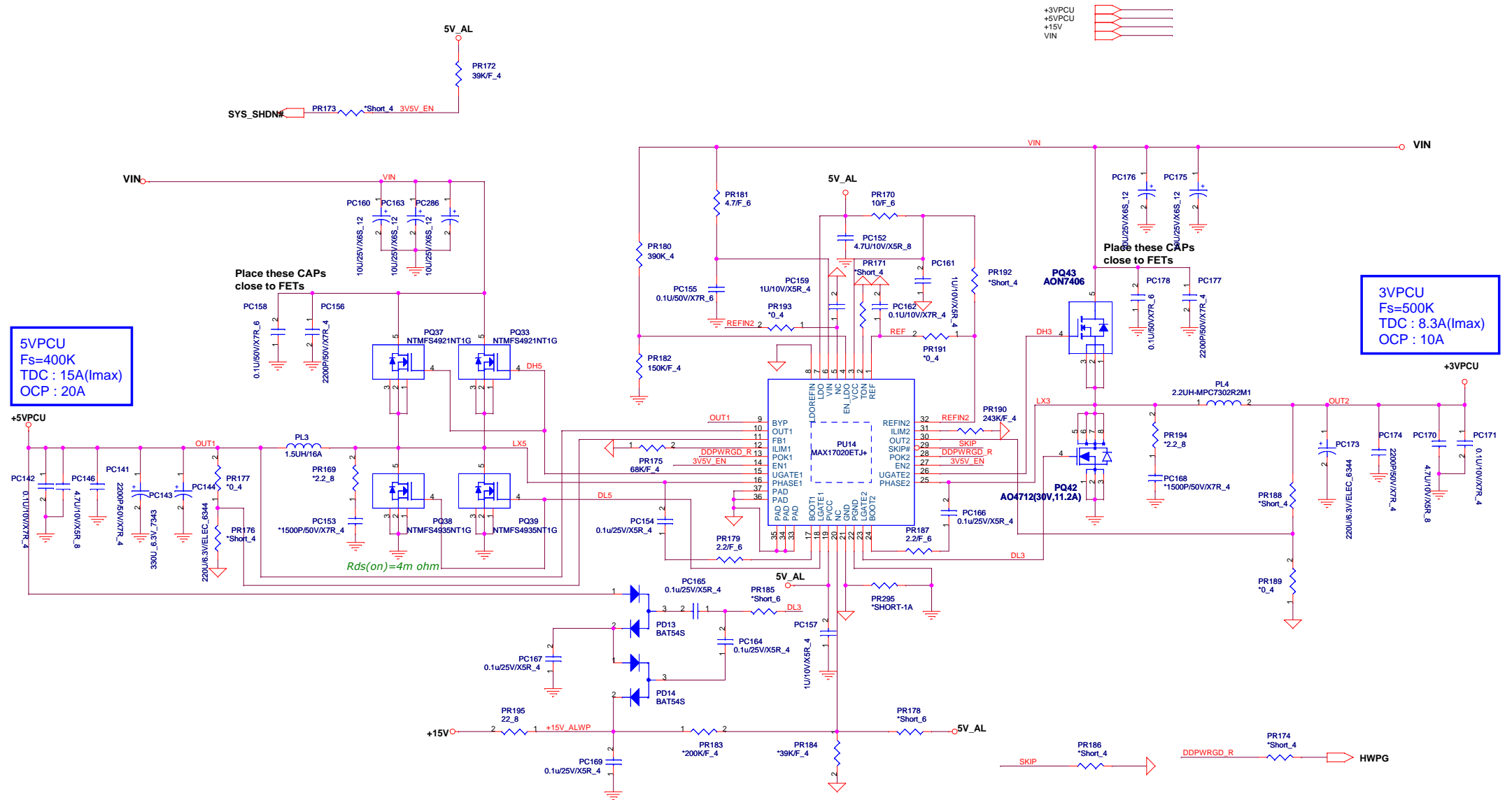
 PROJECT KL3 NOTE Calpella DIS Quanta Computer Inc.		
Size Custom	Document Number HOLD & SKEW	Rev 1A
Date: Thursday, September 30, 2010	Sheet 37	of 48

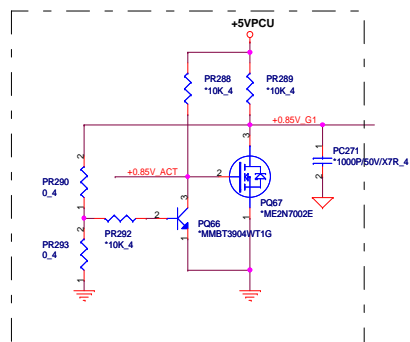
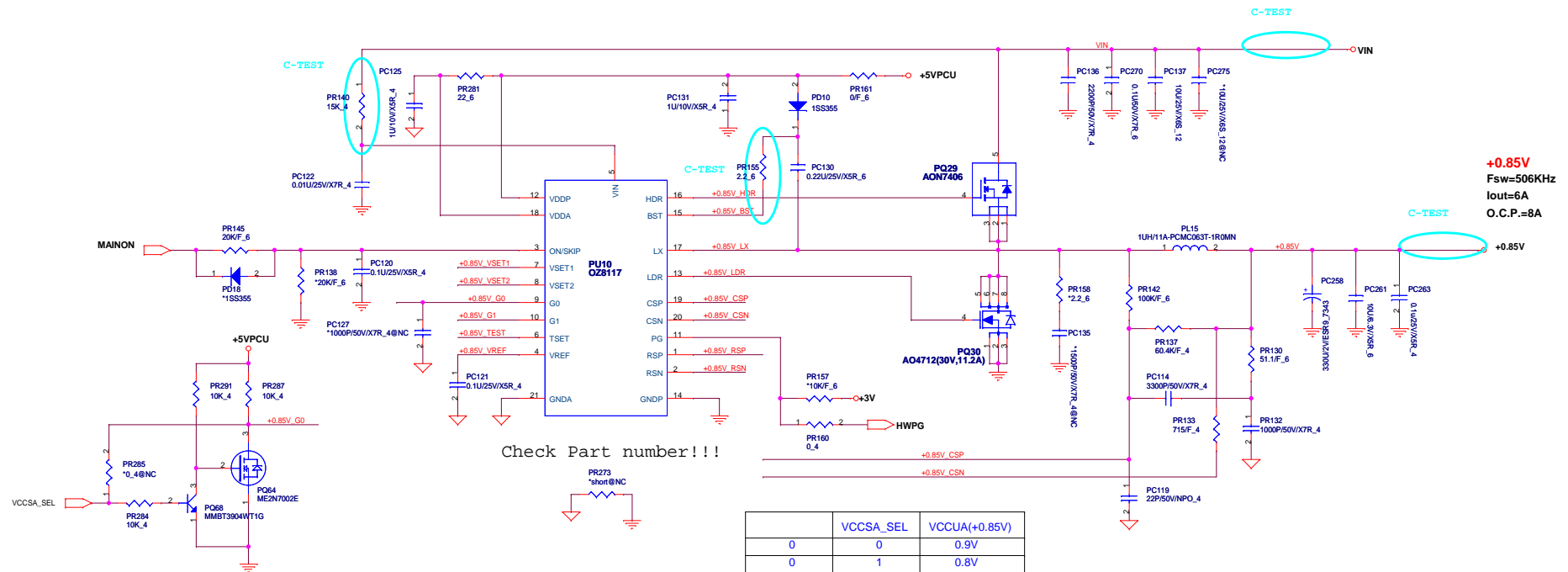




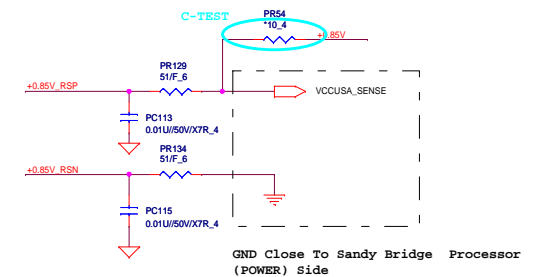
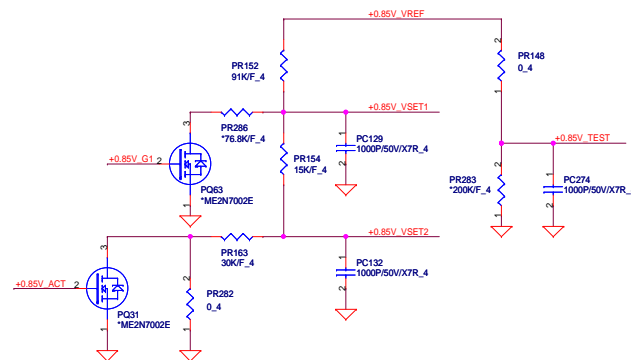


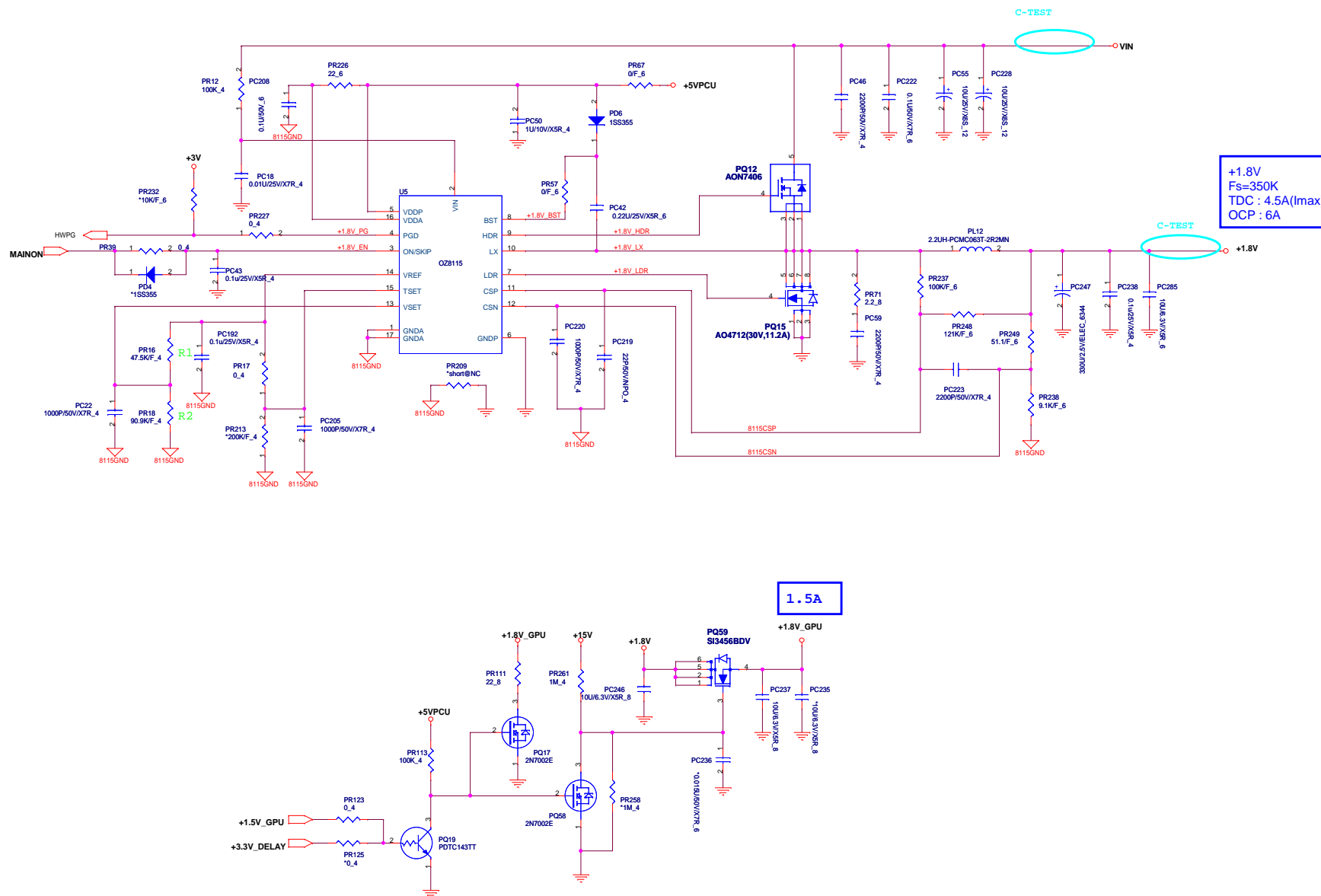


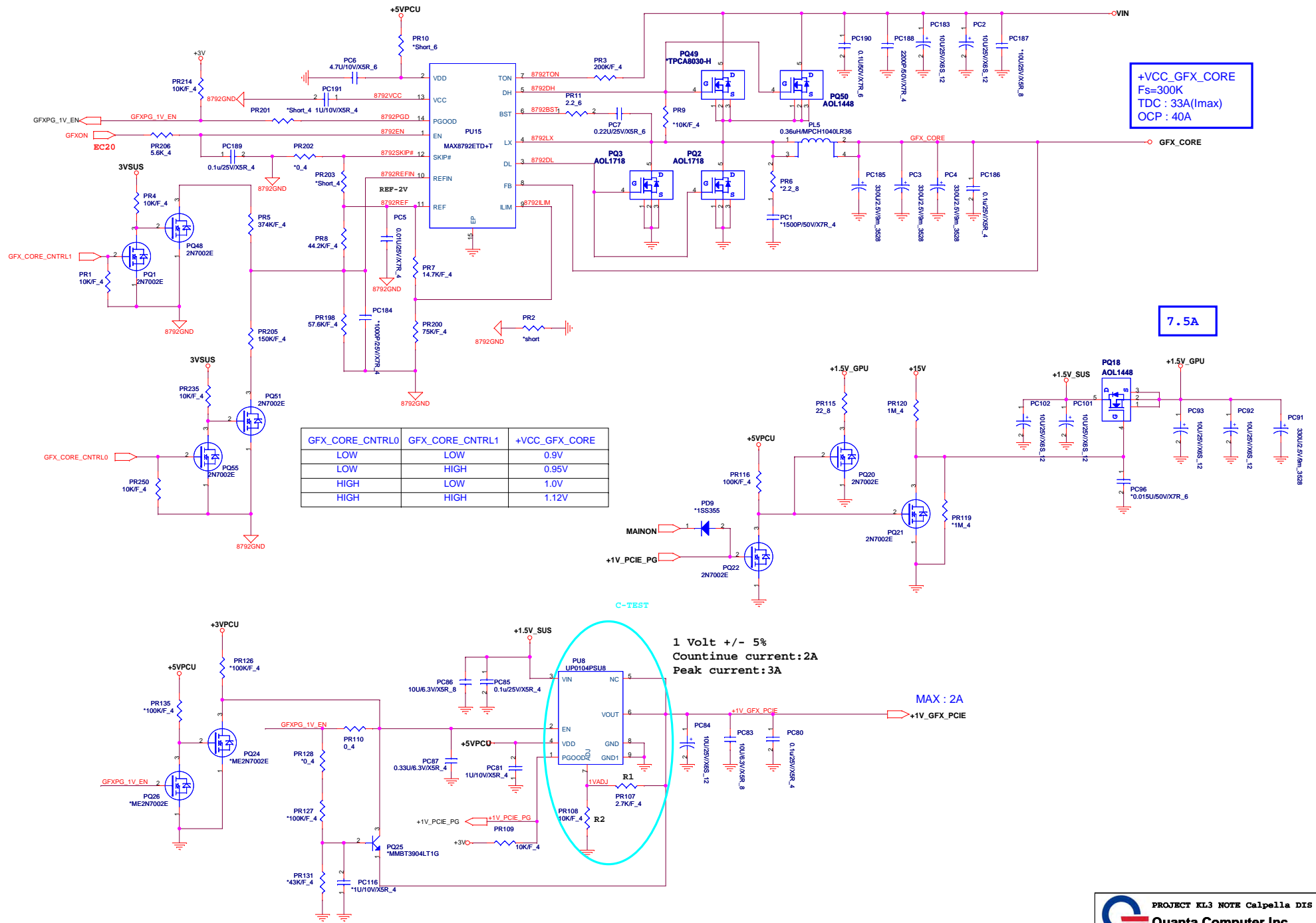


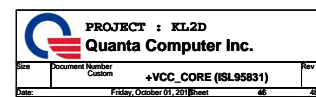


For Sandy Bridge And IV Bridge VID Select

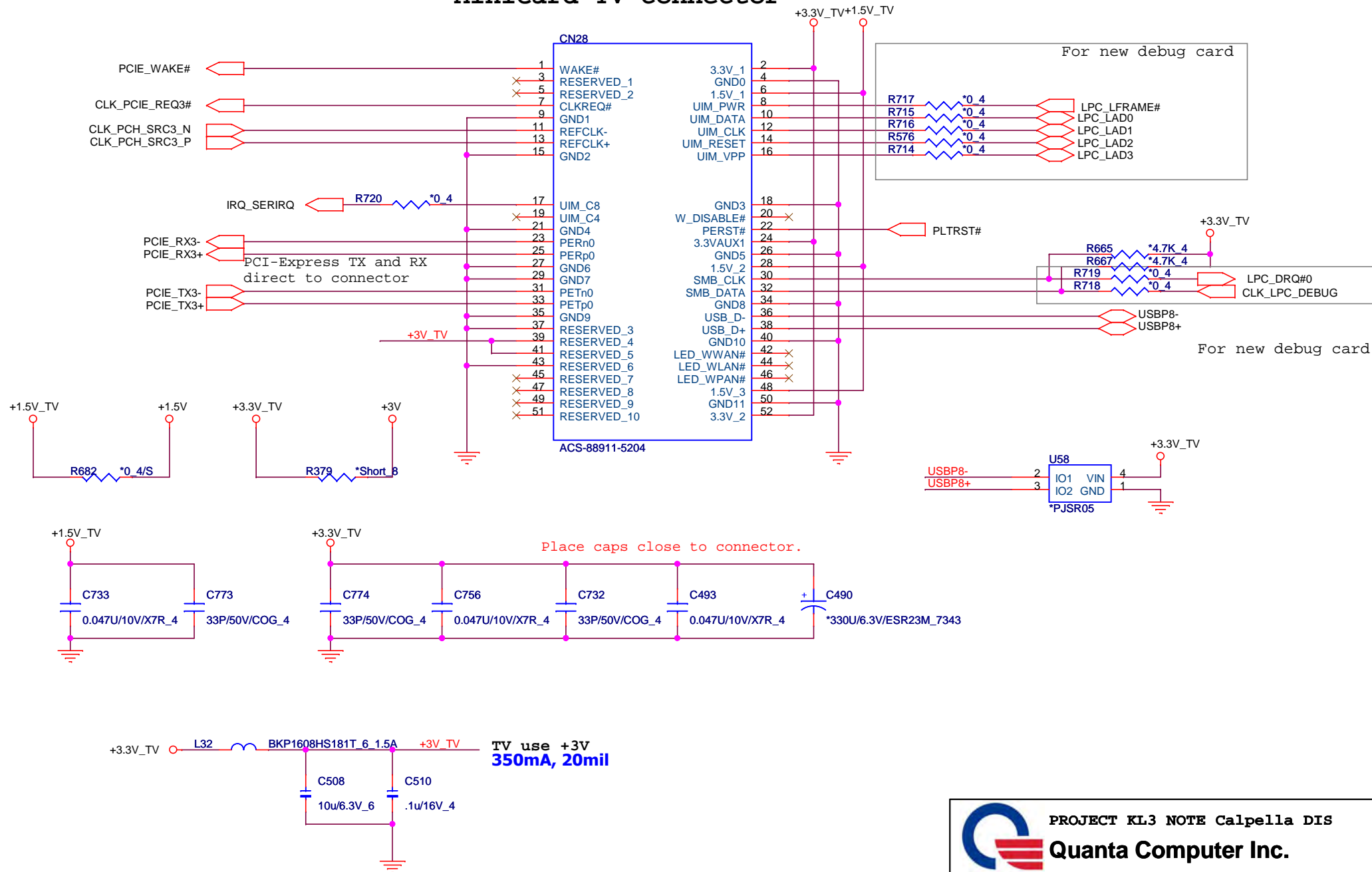




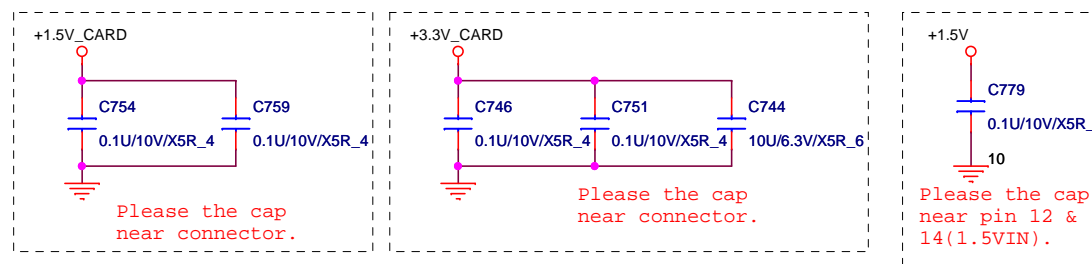
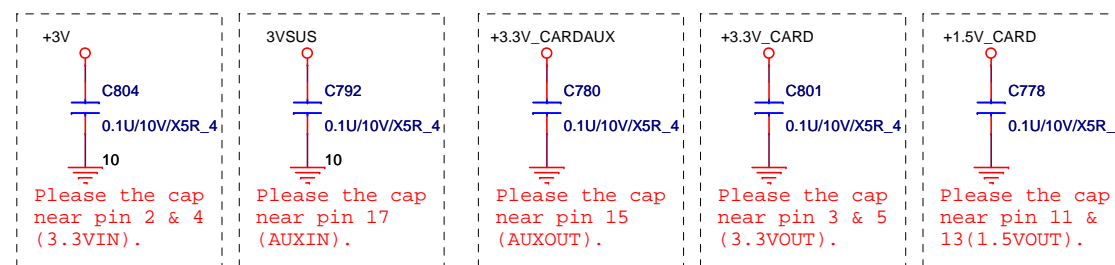
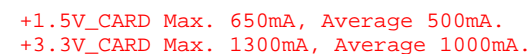




MiniCard TV connector



33



JAE PX10FS16PH-26P

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Date: Thursday, September 30, 2010

Sheet 48 of 48